Digital Integrated Circuits
A Design Perspective

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Introduction

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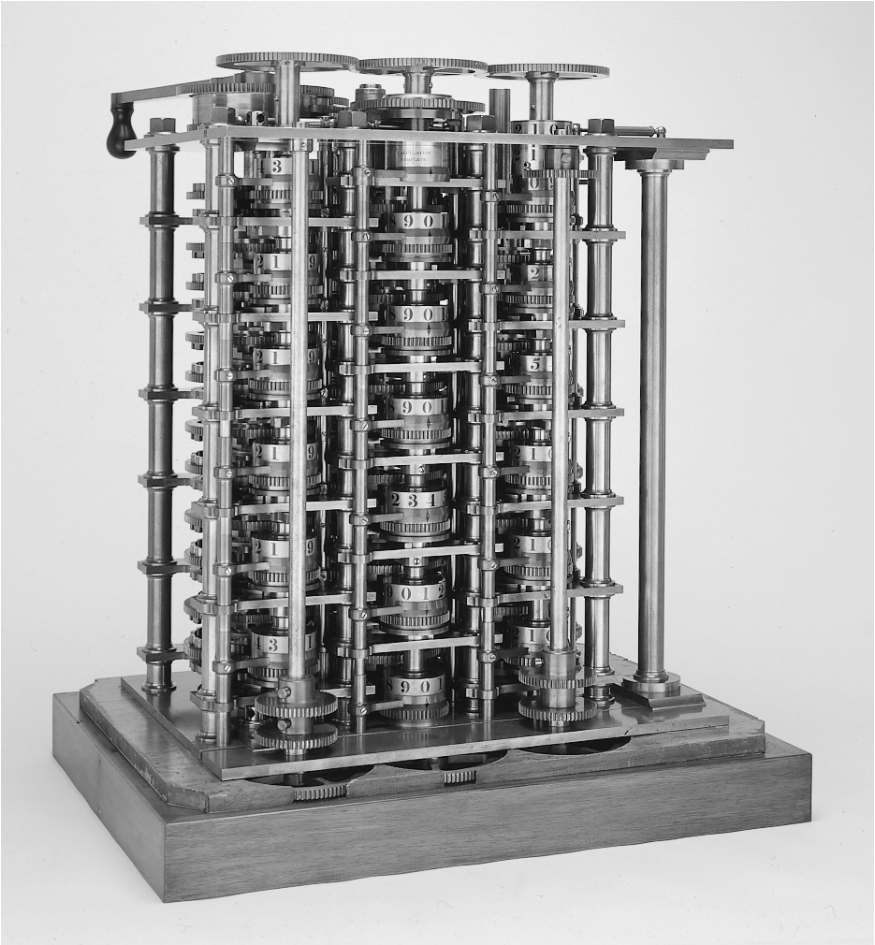
Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

The First Computer



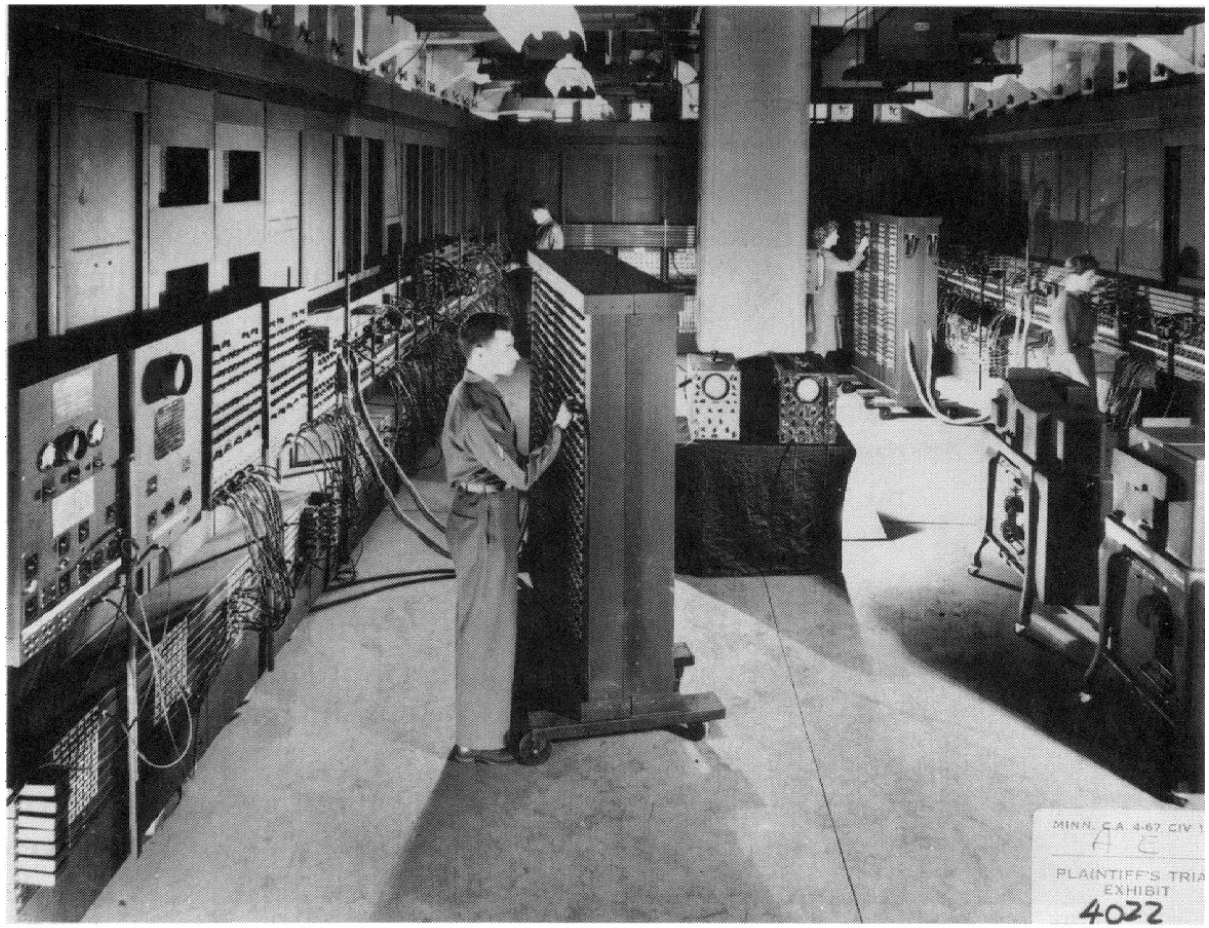
Primo esempio di sistema computazionale meccanico

The Babbage Difference Engine (1832)

25,000 parts

cost: £17,470

ENIAC - The first electronic computer (1946)

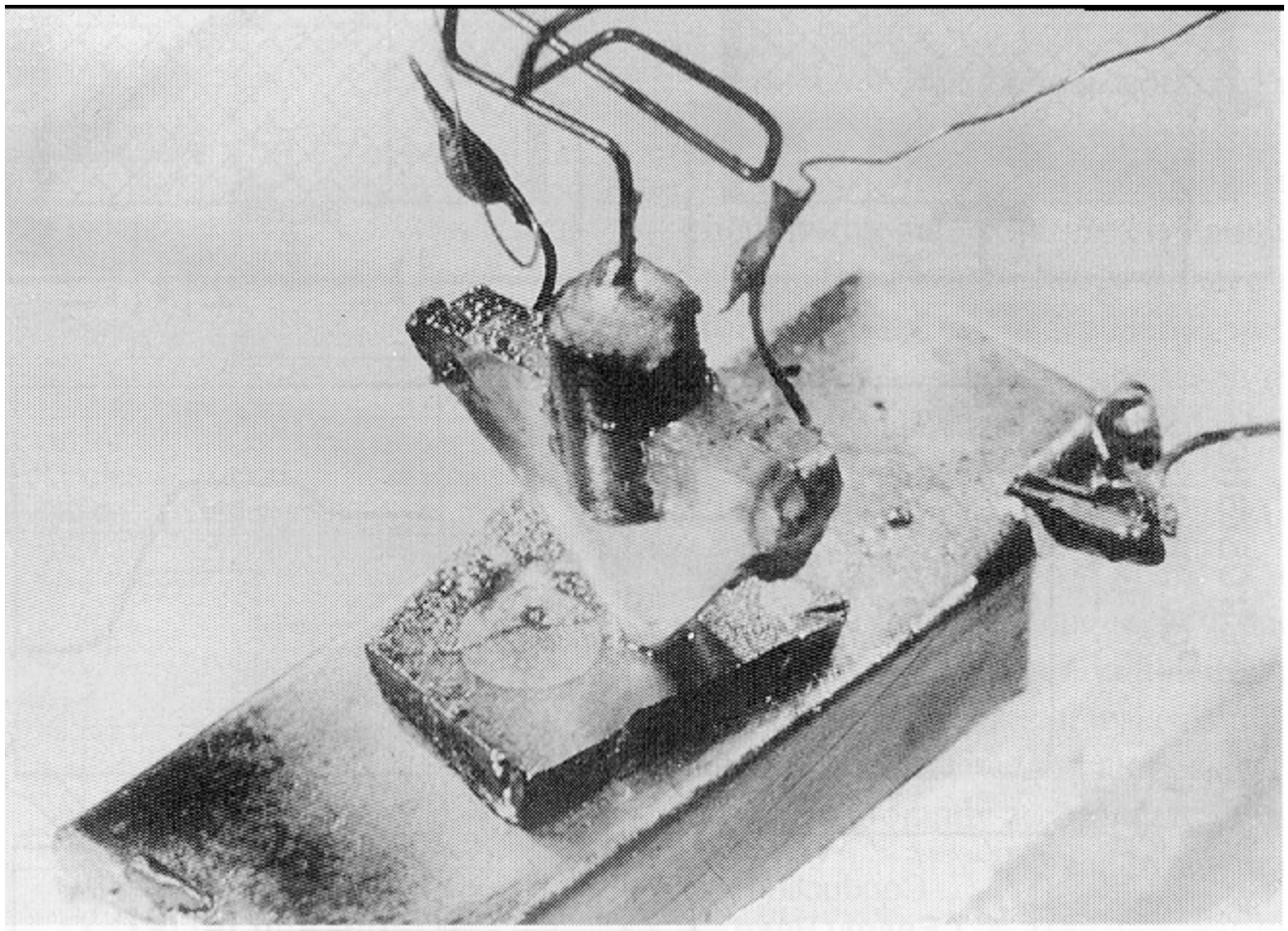


L=24m

H=2.6m

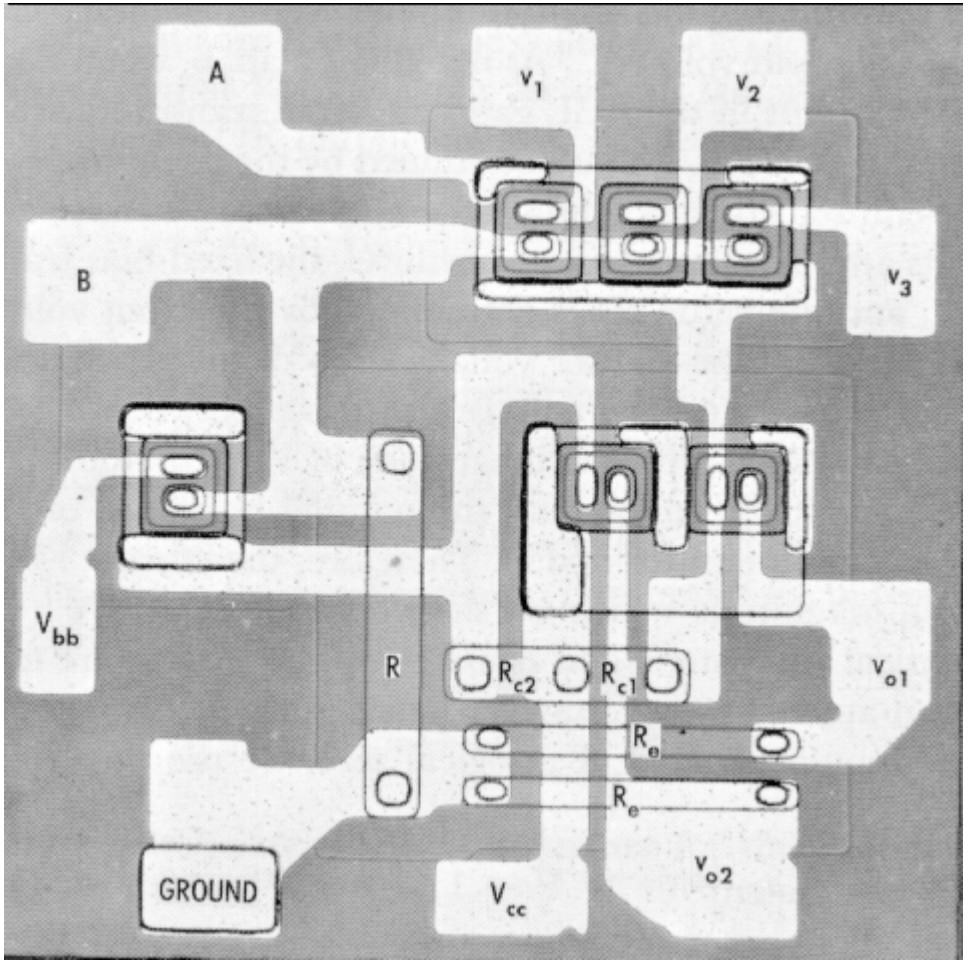
18000 Valvole

The Transistor Revolution



First transistor
Bell Labs, 1948

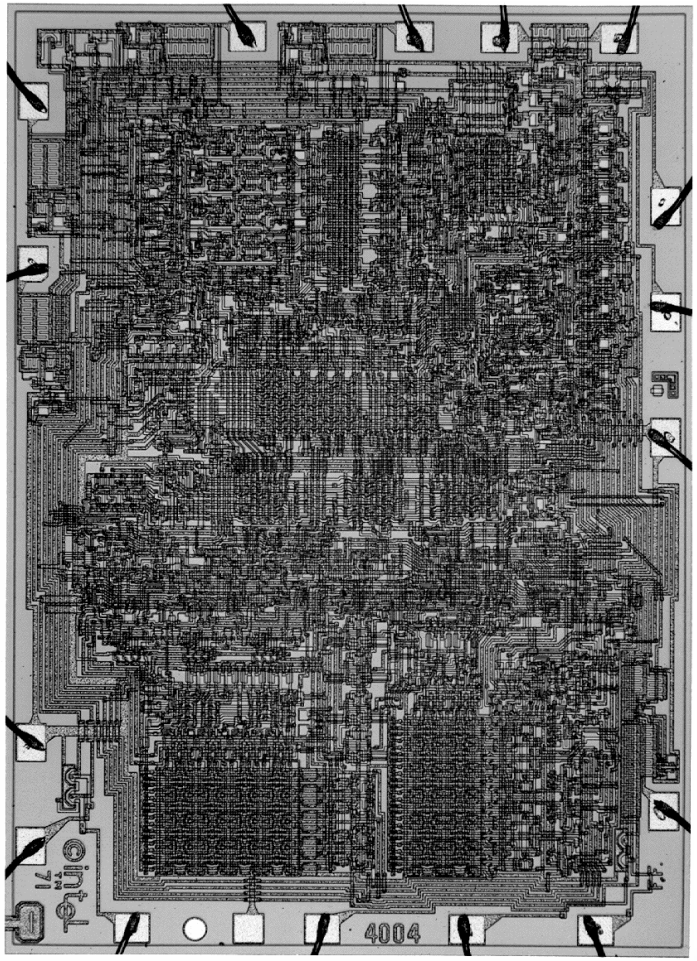
The First Integrated Circuits



Bipolar logic
1960's

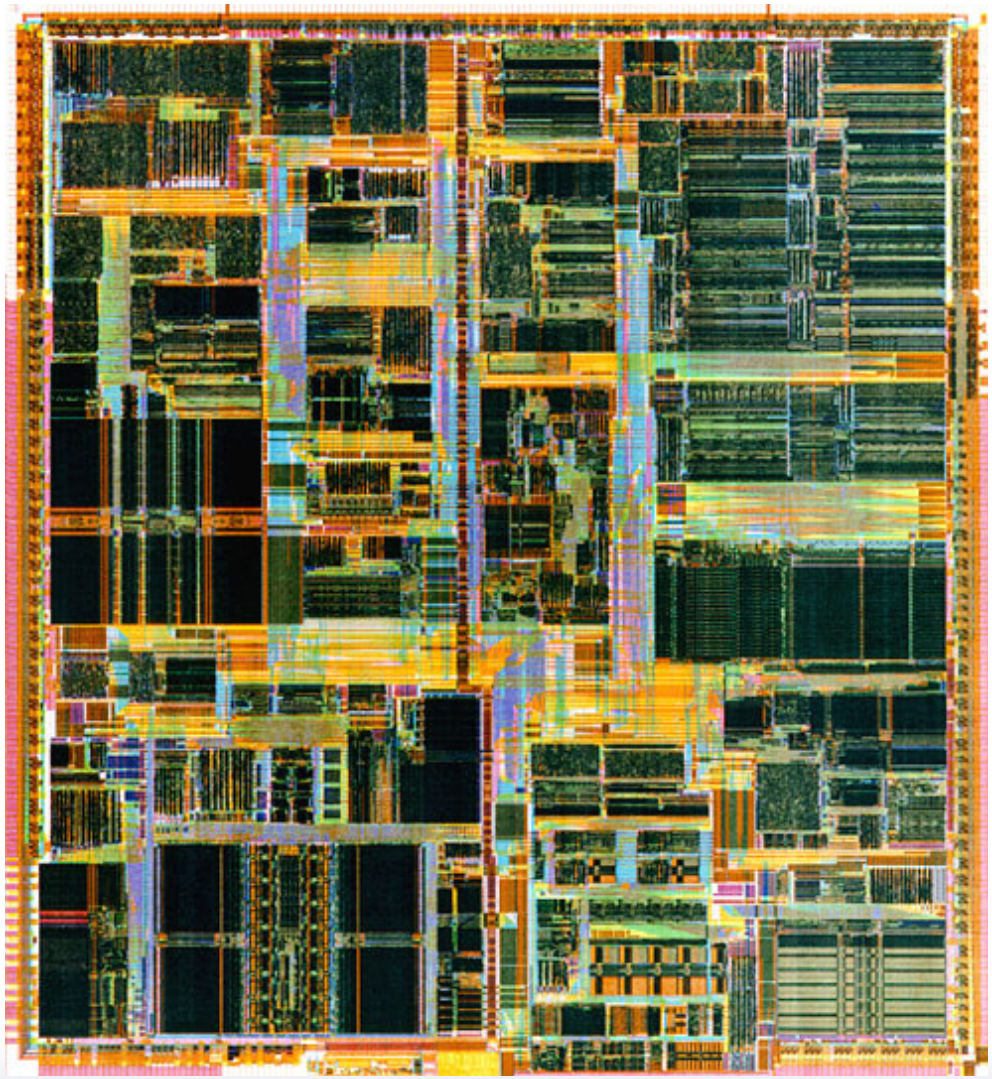
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



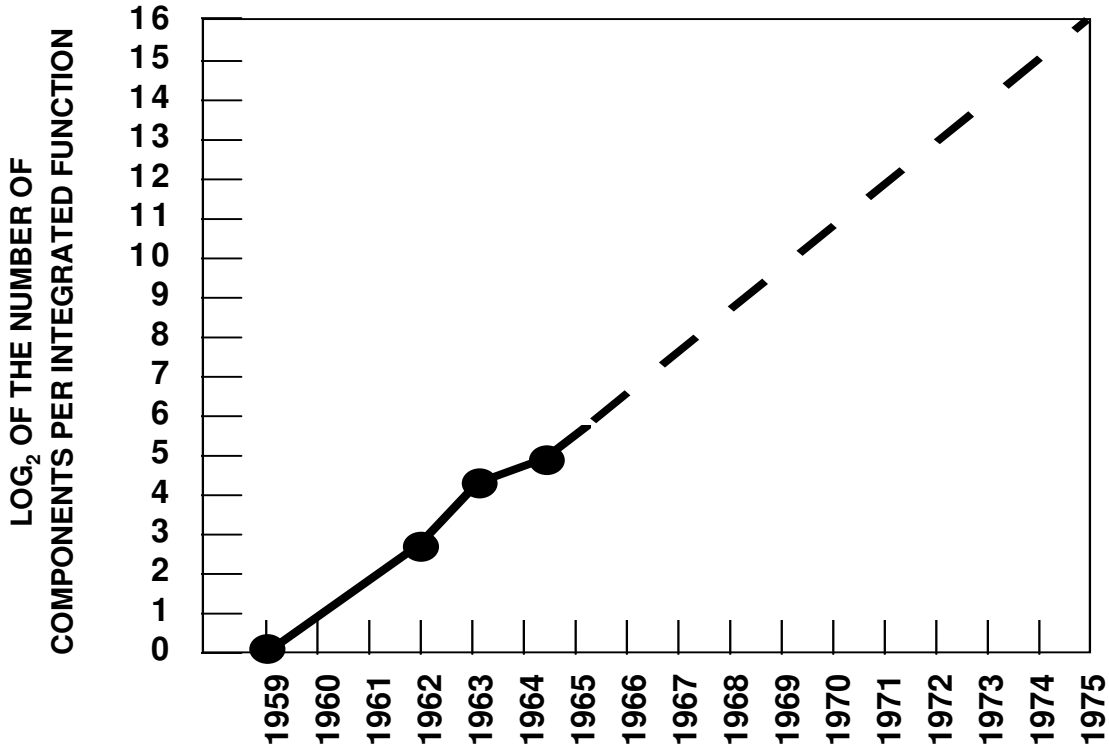
Moore's Law

"La densità di componenti è raddoppiata ogni anno. Sicuramente, a breve termine ci si può attendere che questo ritmo continui, o addirittura acceleri. Nel lungo periodo, la velocità è meno prevedibile, sebbene non vi sia alcuna ragione per credere che questo ritmo non debba rimanere circa costante per almeno dieci anni. Ciò significa che nel 1975, il numero di componenti per circuito integrato sarà 65.000"

Moore's Law

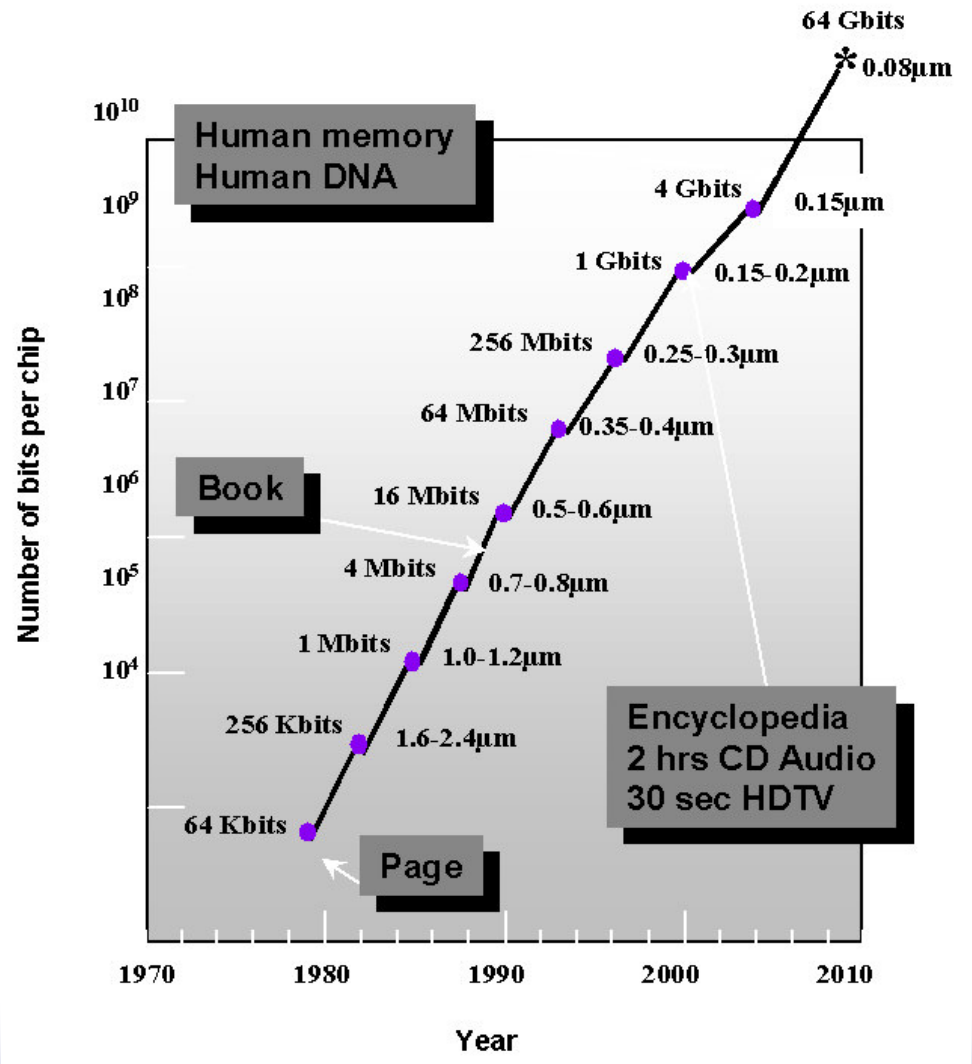
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

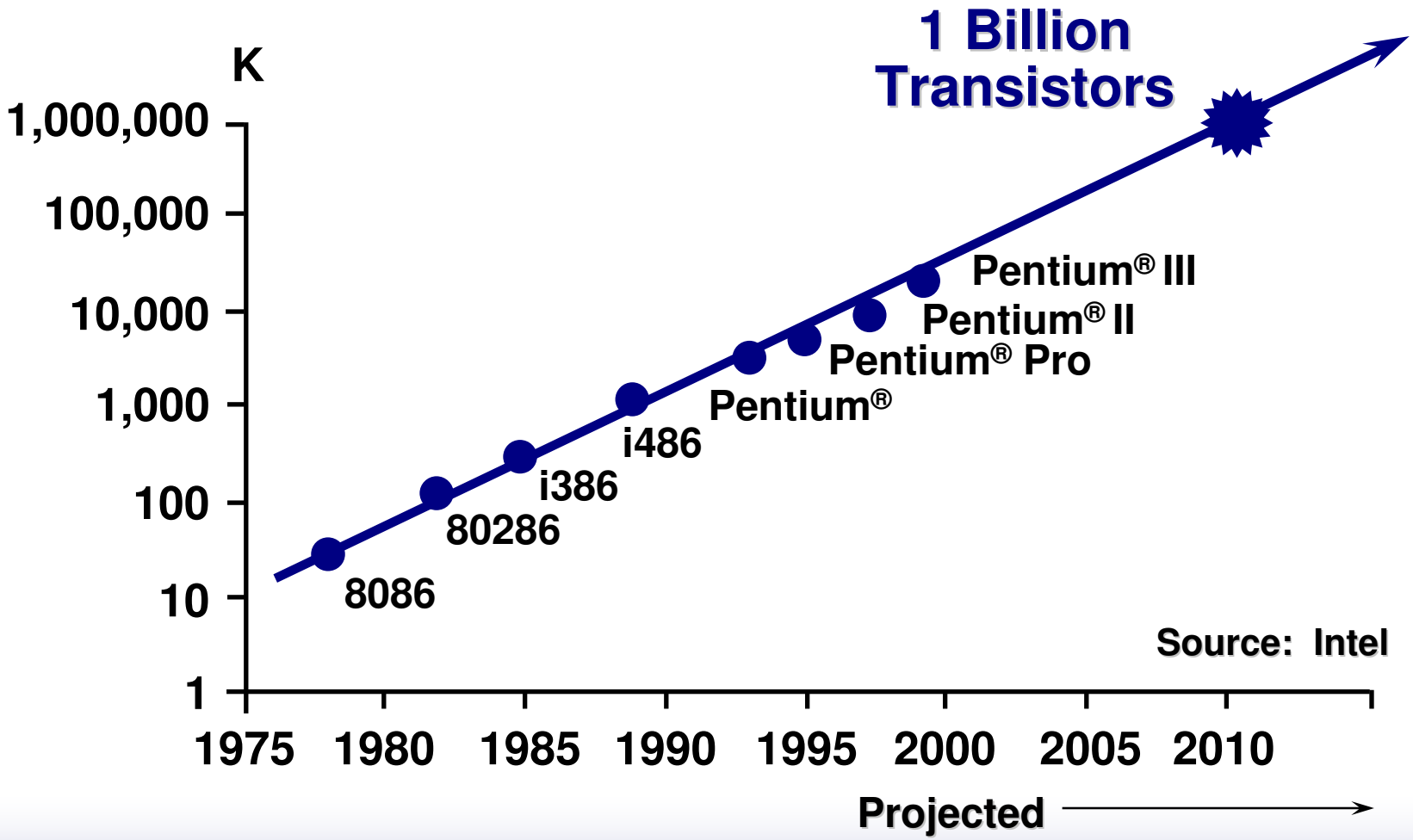


Electronics, April 19, 1965.

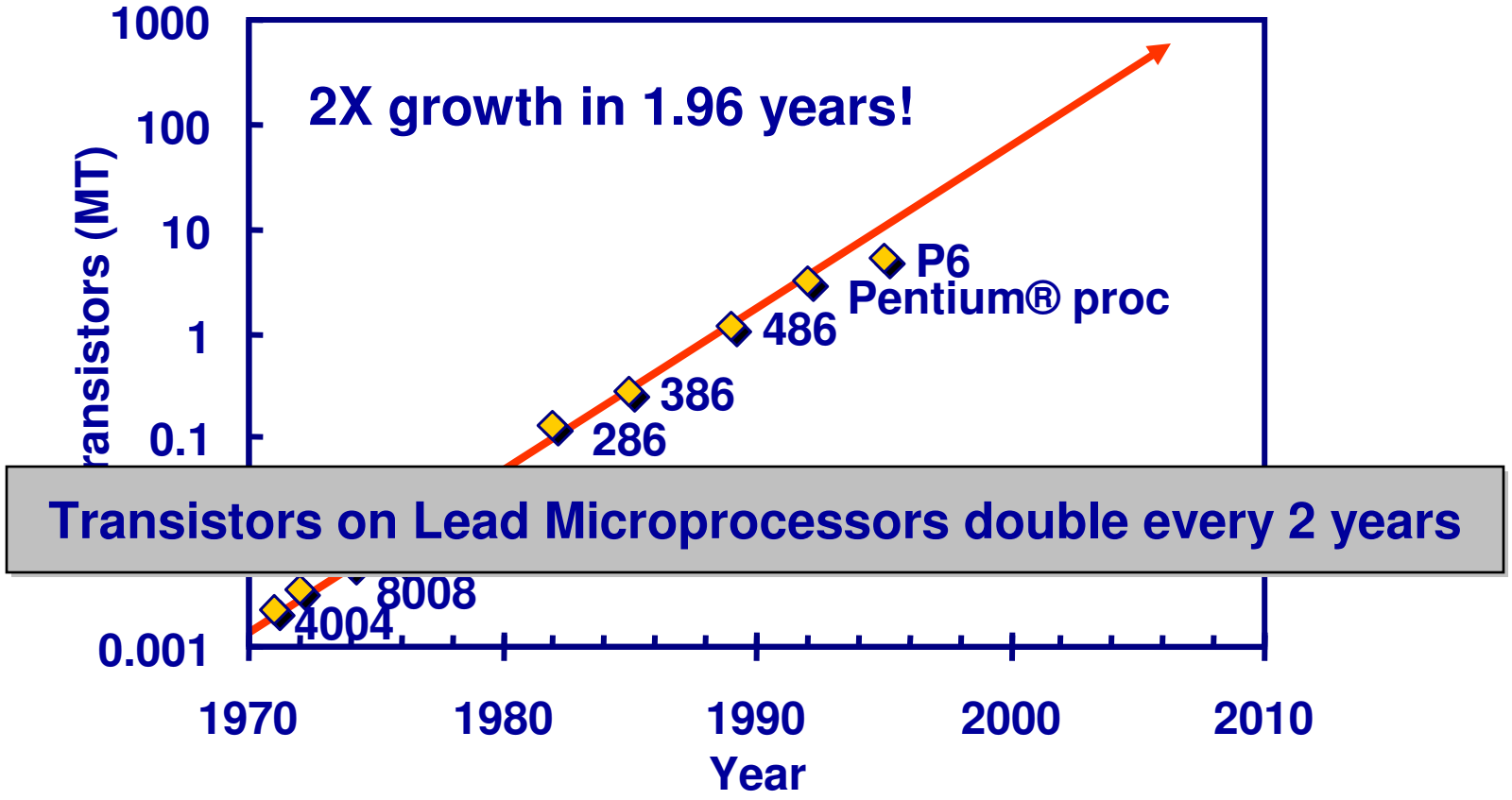
Evolution in Complexity



Transistor Counts

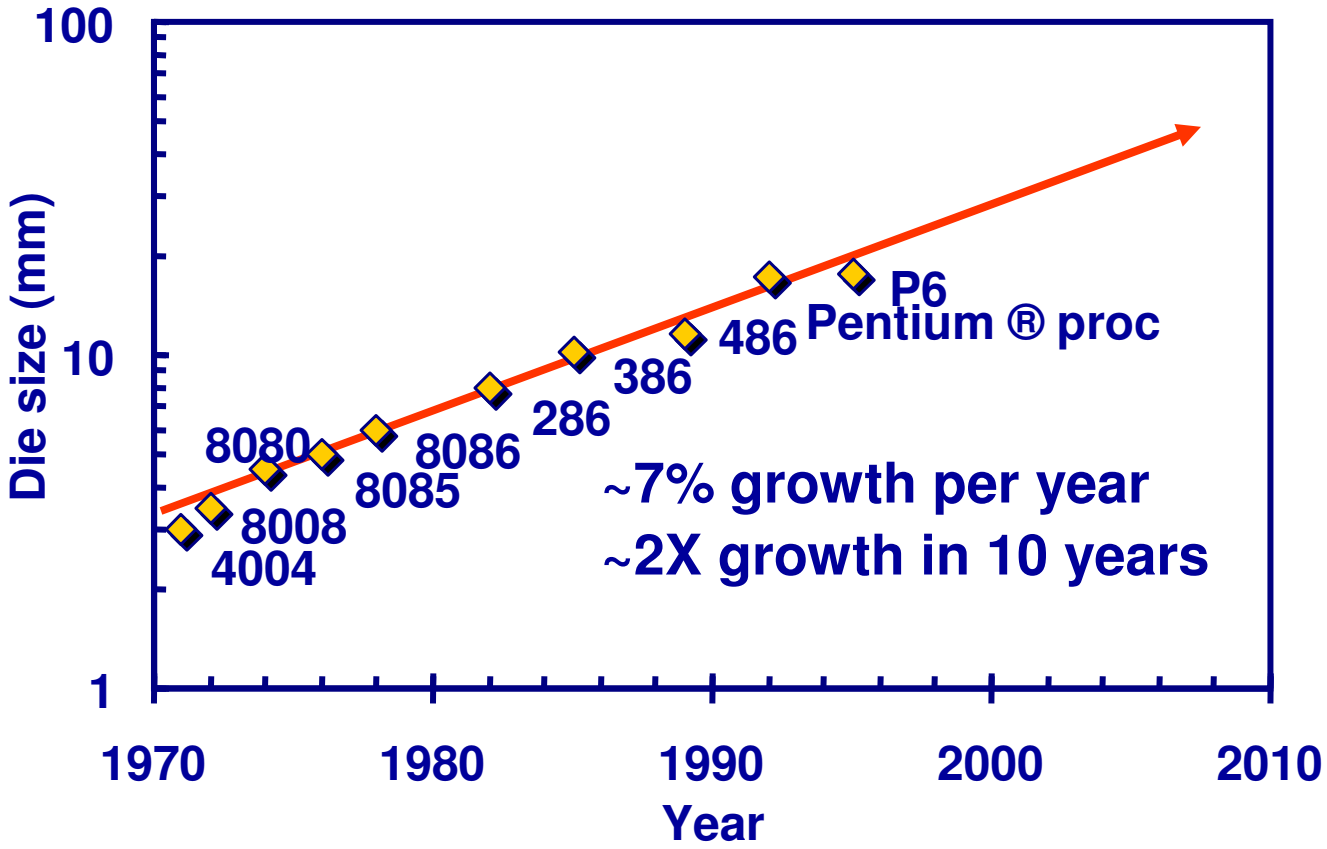


Moore's law in Microprocessors



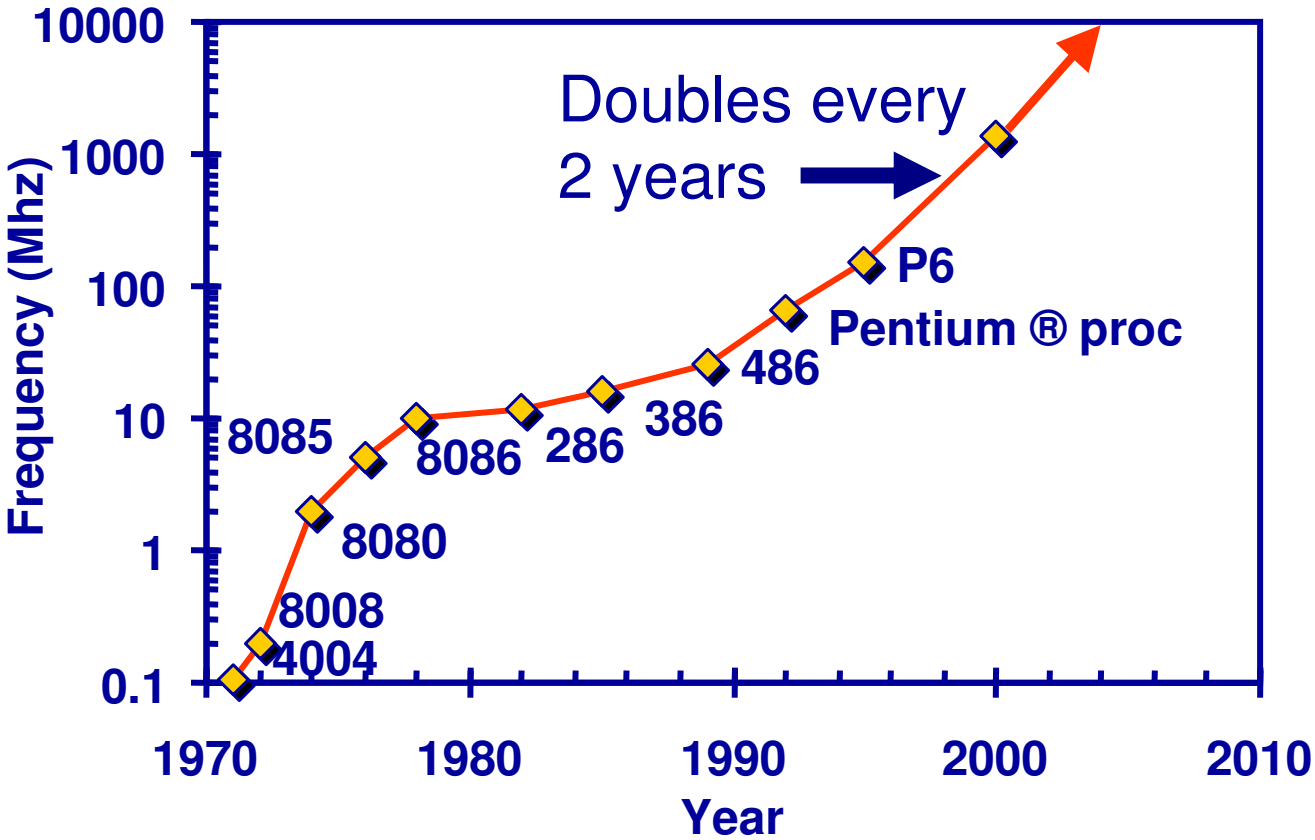
Transistors on Lead Microprocessors double every 2 years

Die Size Growth



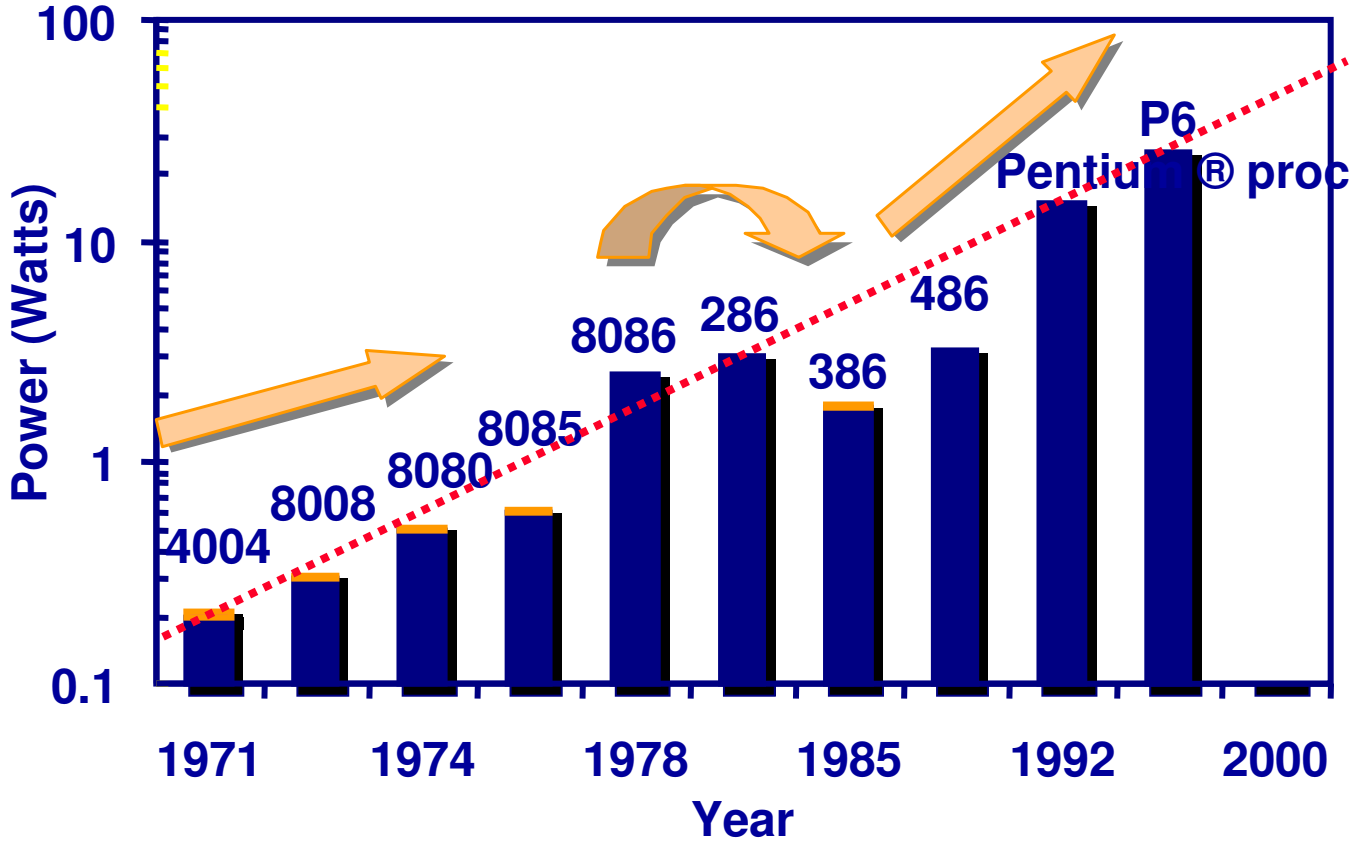
Die size grows by 14% to satisfy Moore's Law

Frequency



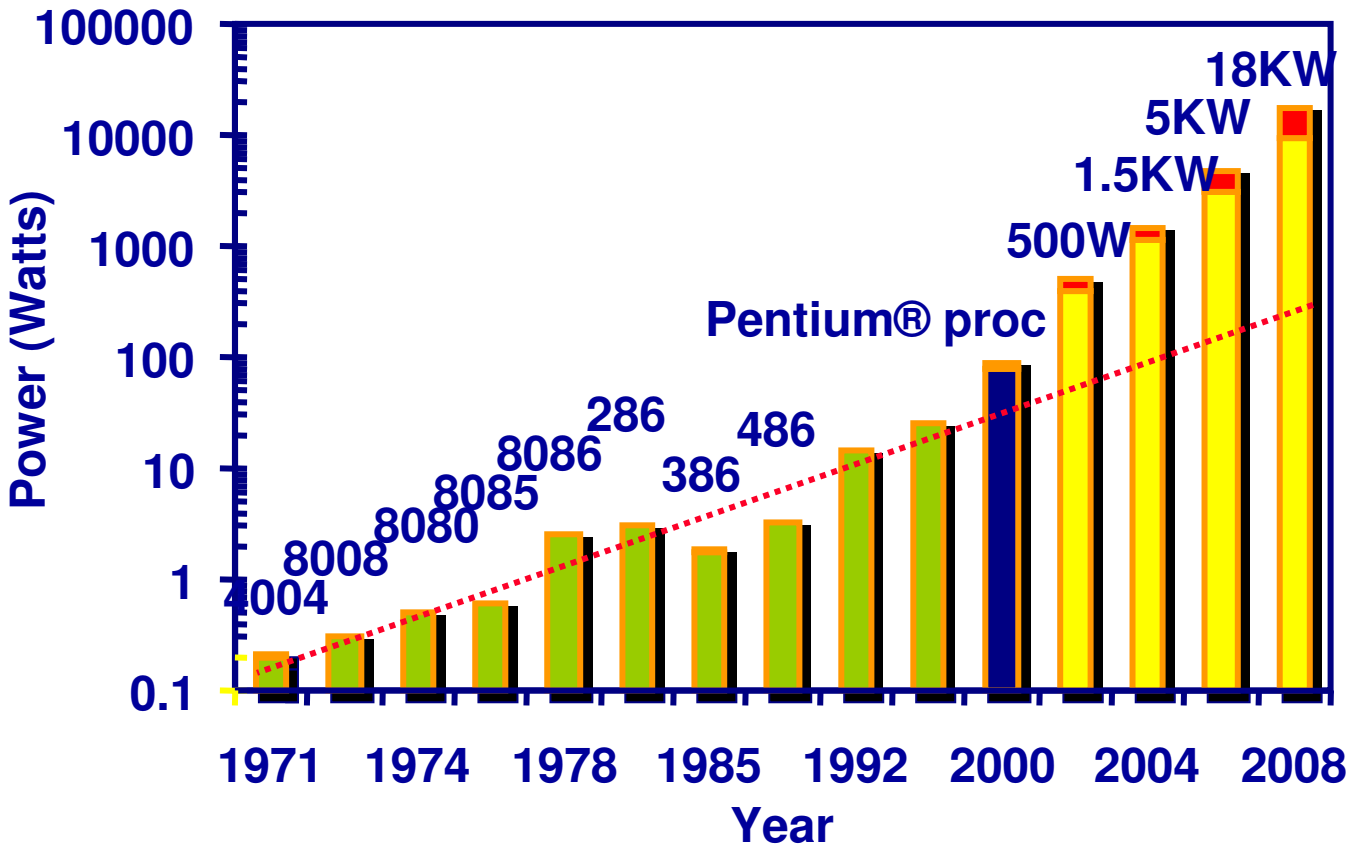
Lead Microprocessors frequency doubles every 2 years

Power Dissipation



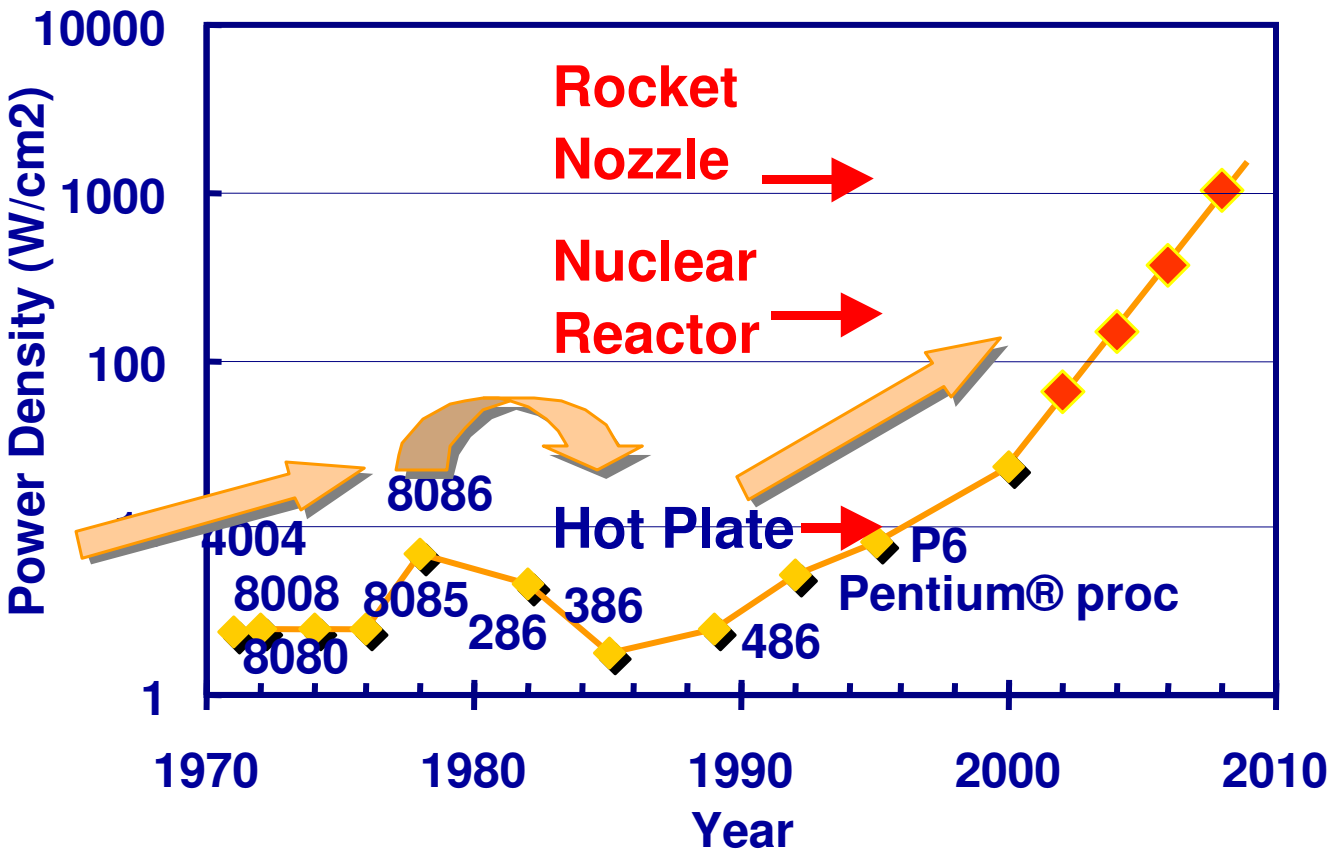
Lead Microprocessors power continues to increase

Power will be a major problem



Power delivery and dissipation will be prohibitive

Power density



Power density too high to keep junctions at low temp

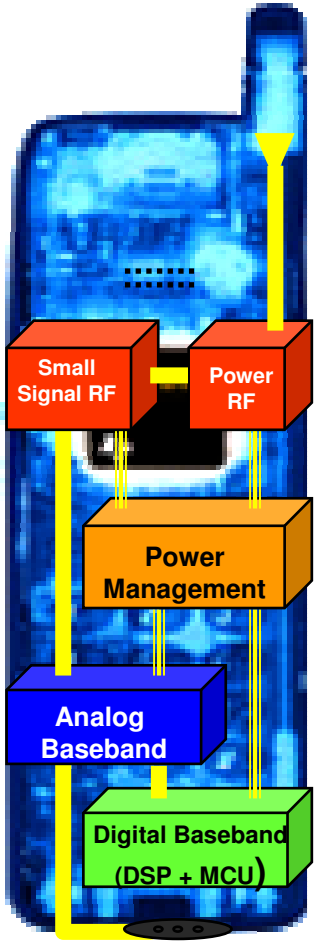
Not Only Microprocessors

Cell
Phone

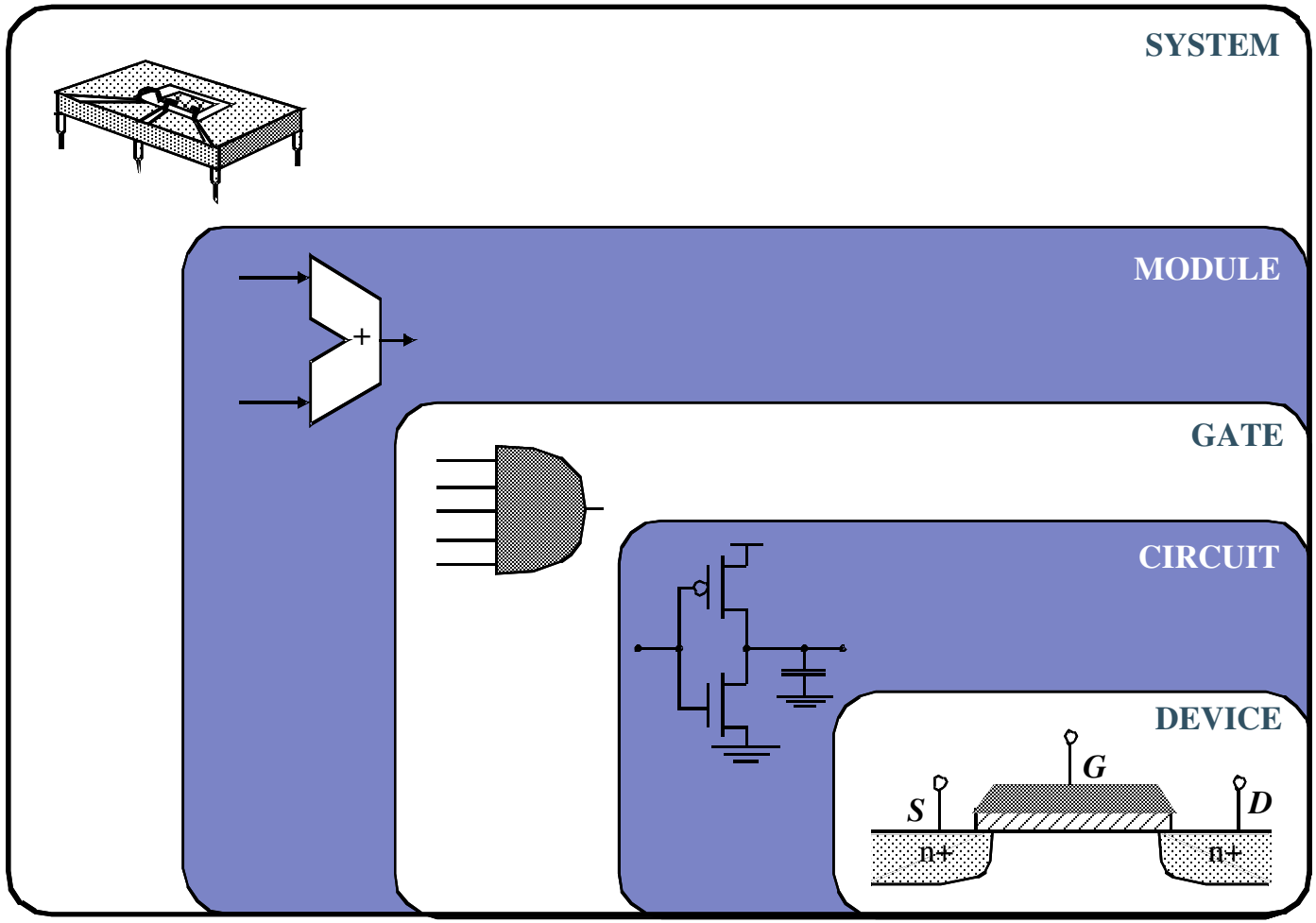
Digital Cellular Market
(Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Design Abstraction Levels



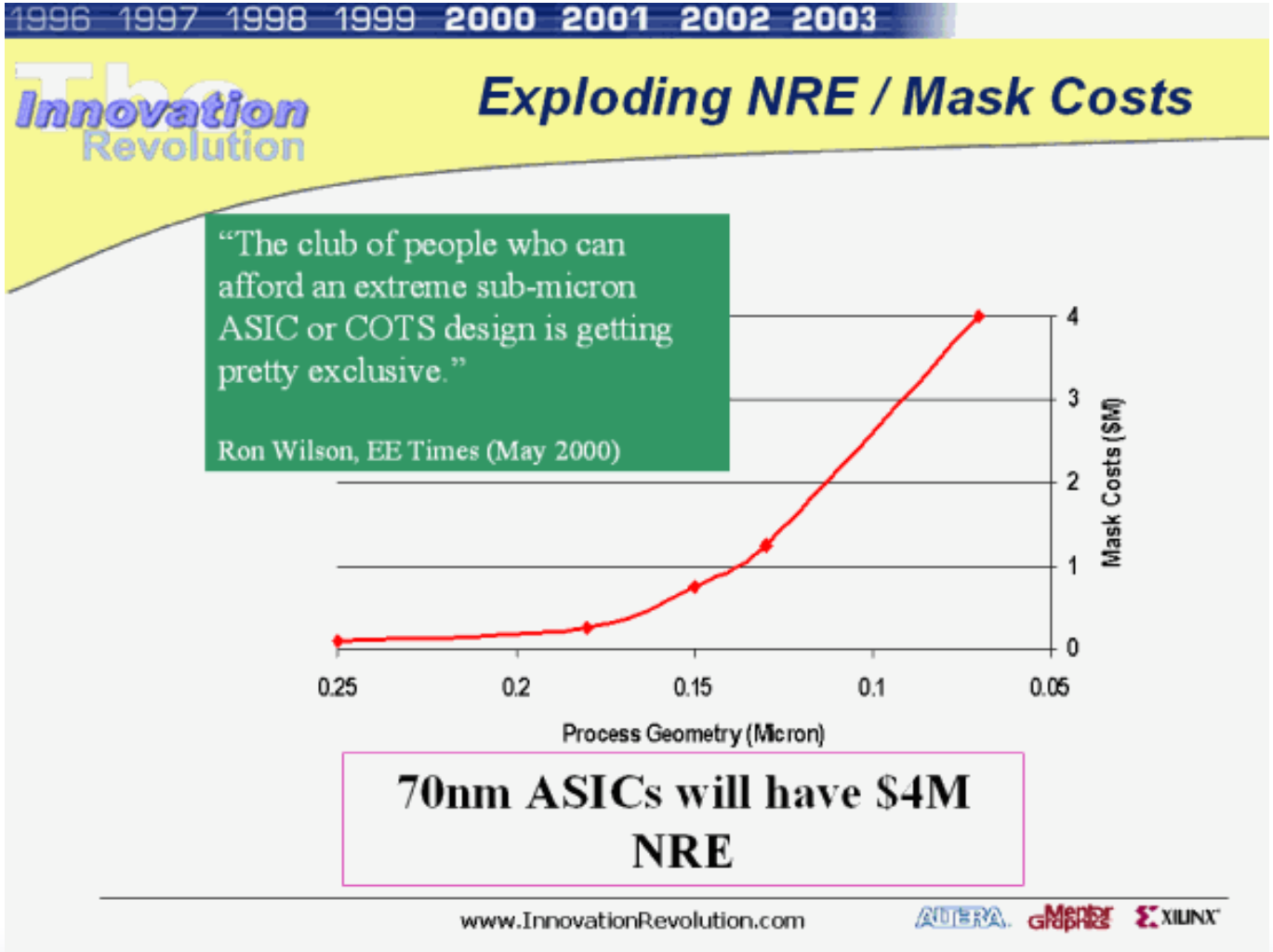
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

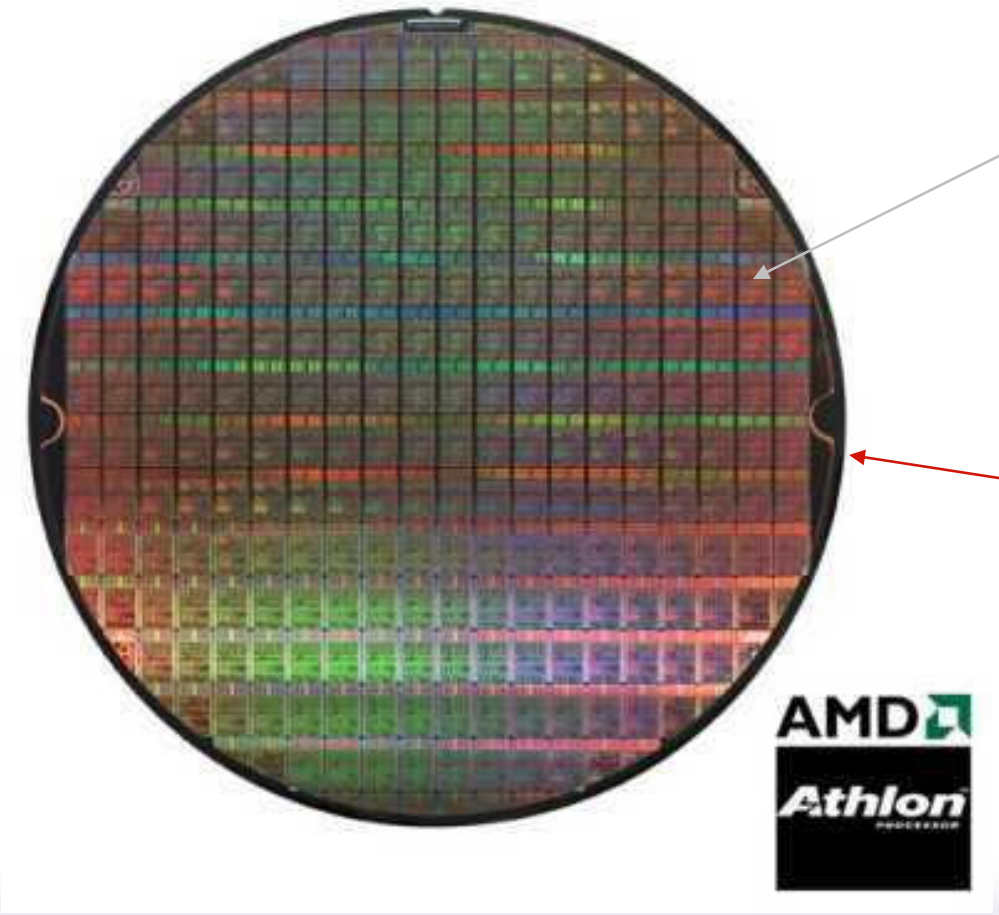
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

NRE Cost is Increasing



Die Cost



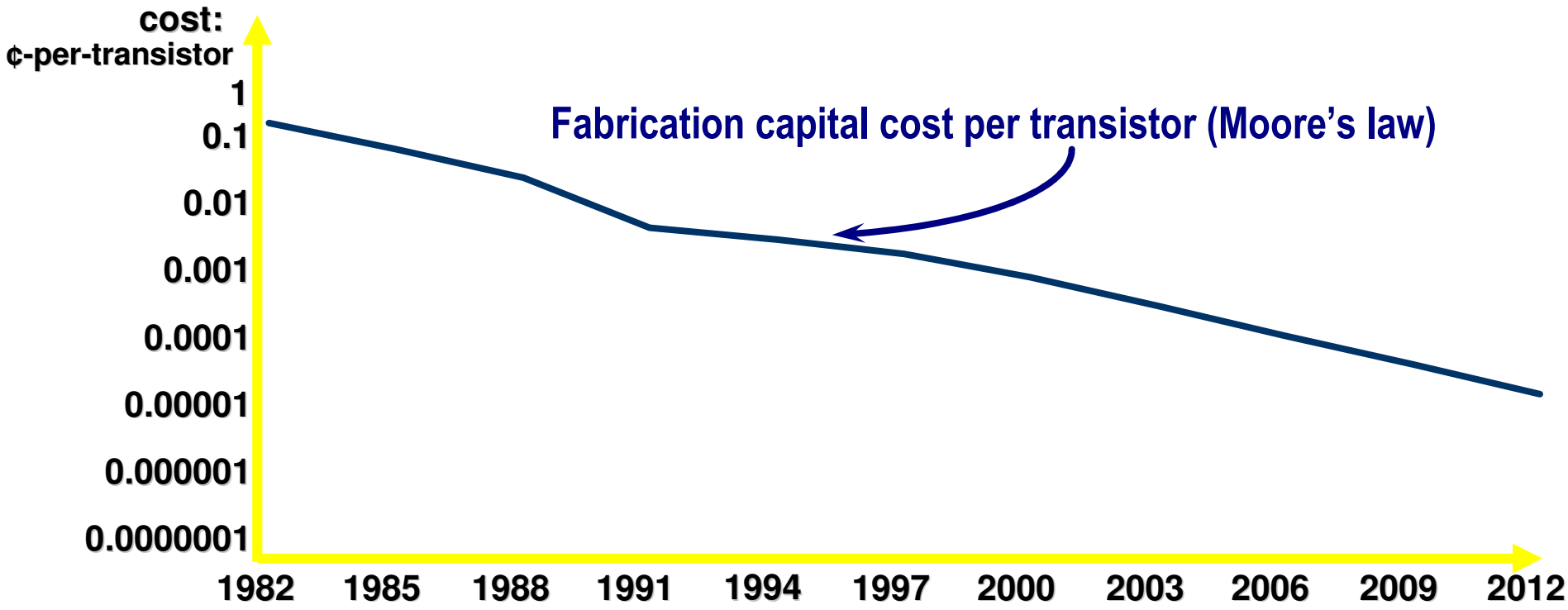
Single die

Wafer

Going up to 12" (30cm)

From http://www.amd.com

Cost per Transistor

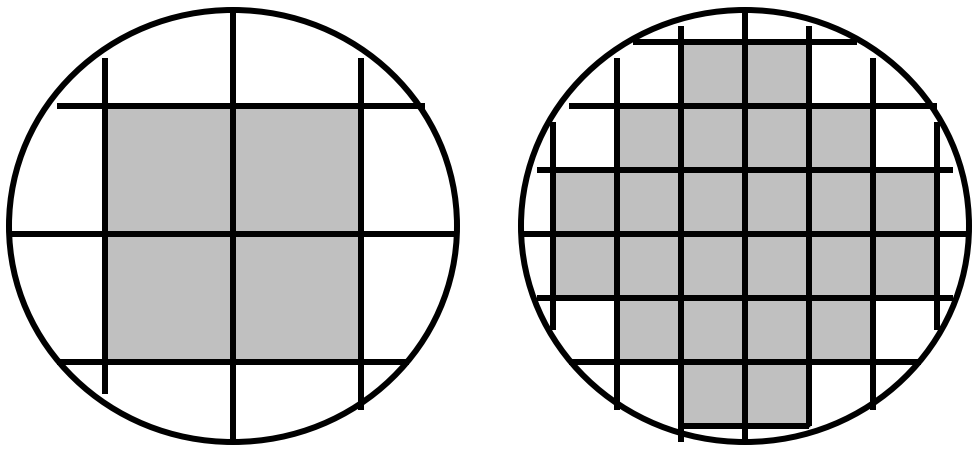


Yield

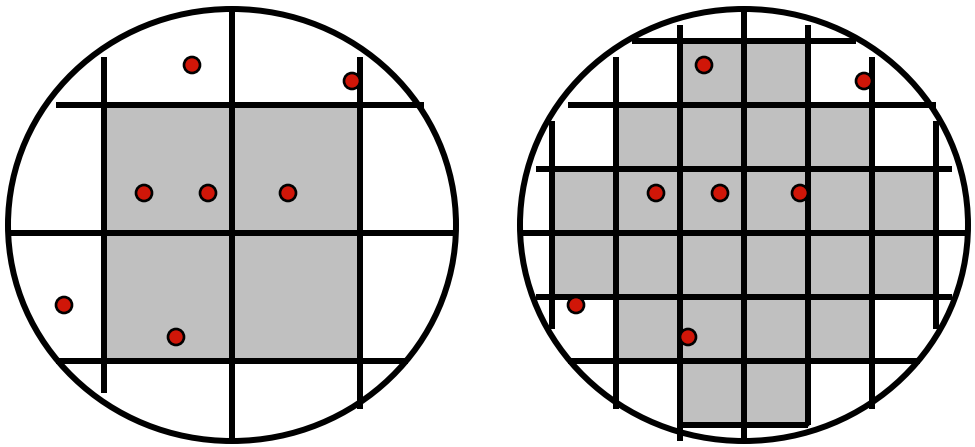
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

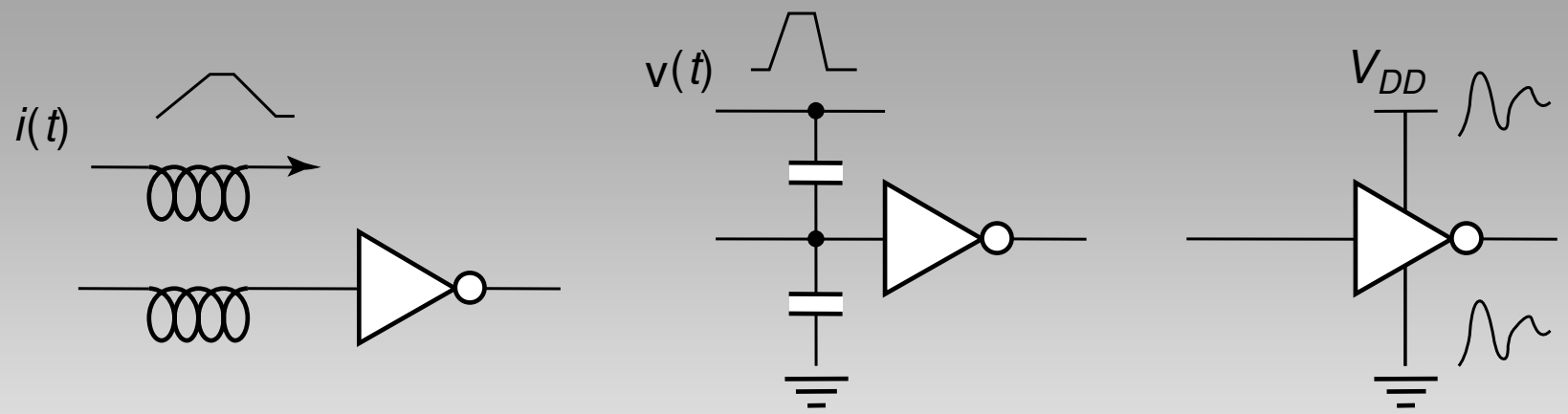
α is approximately 3

$$\text{die cost} = f\,(\text{die area})^4$$

Some Examples (1994)

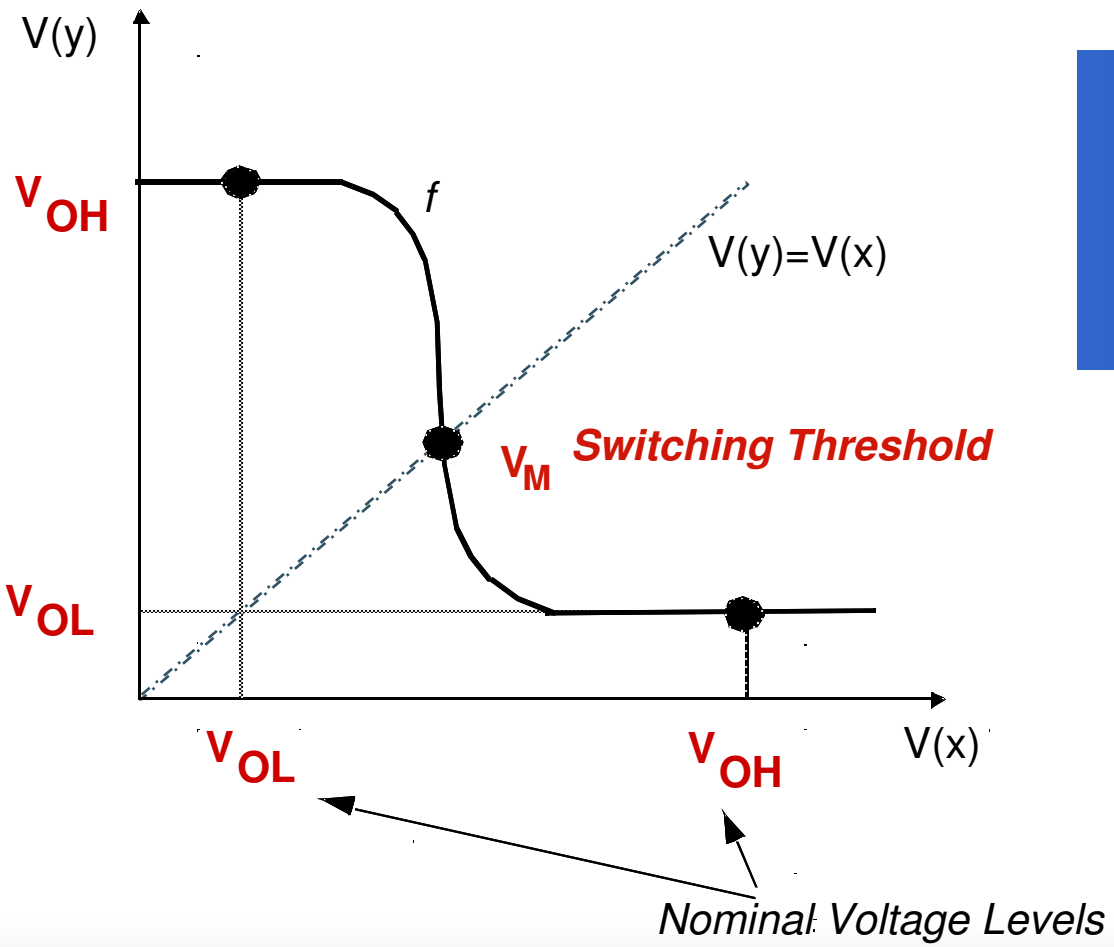
Chip	Metal layers	Line width	Wafer cost	Def./ cm^2	Area mm^2	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability—
Noise in Digital Integrated Circuits



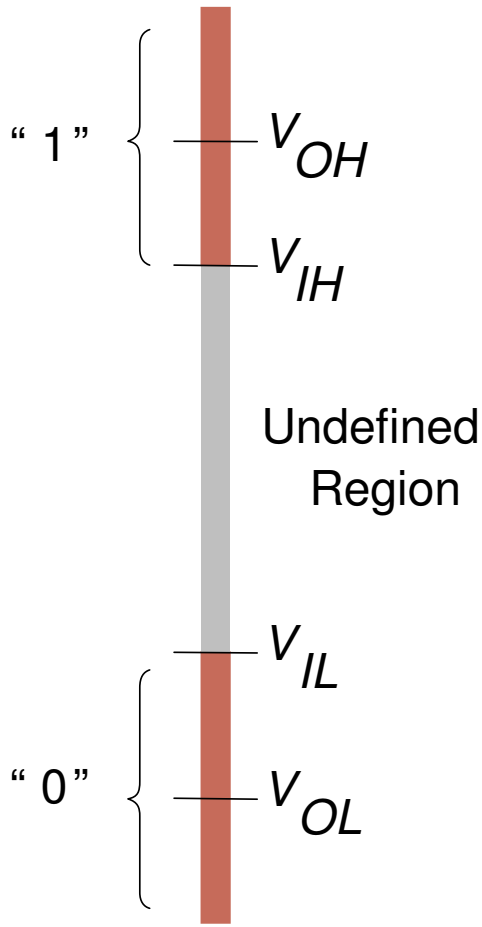
Inductive coupling **Capacitive coupling** **Power and ground noise**

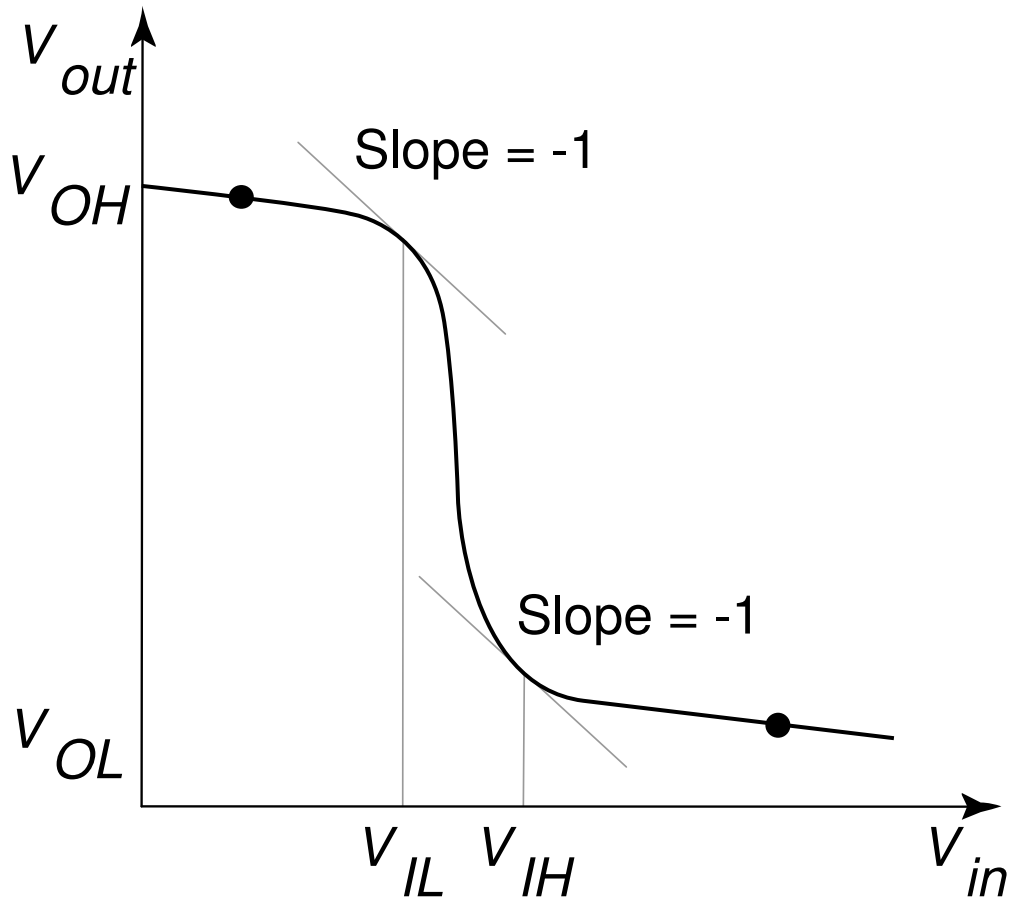
DC Operation
Voltage Transfer Characteristic



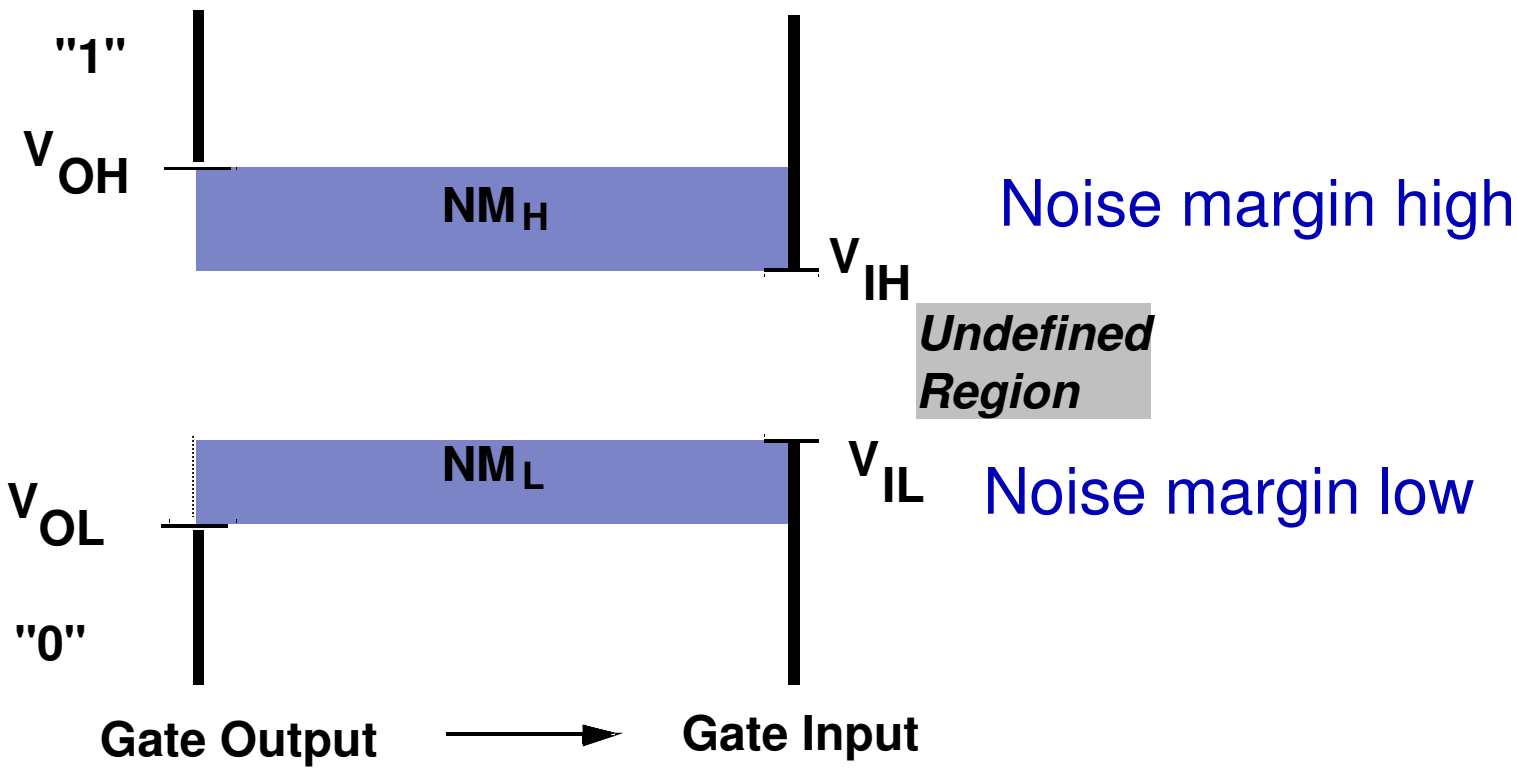
VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Mapping between analog and digital signals

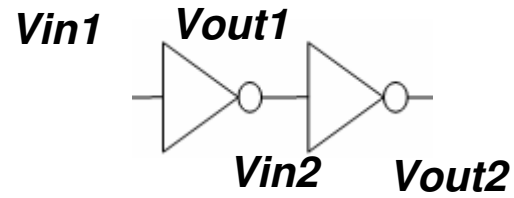


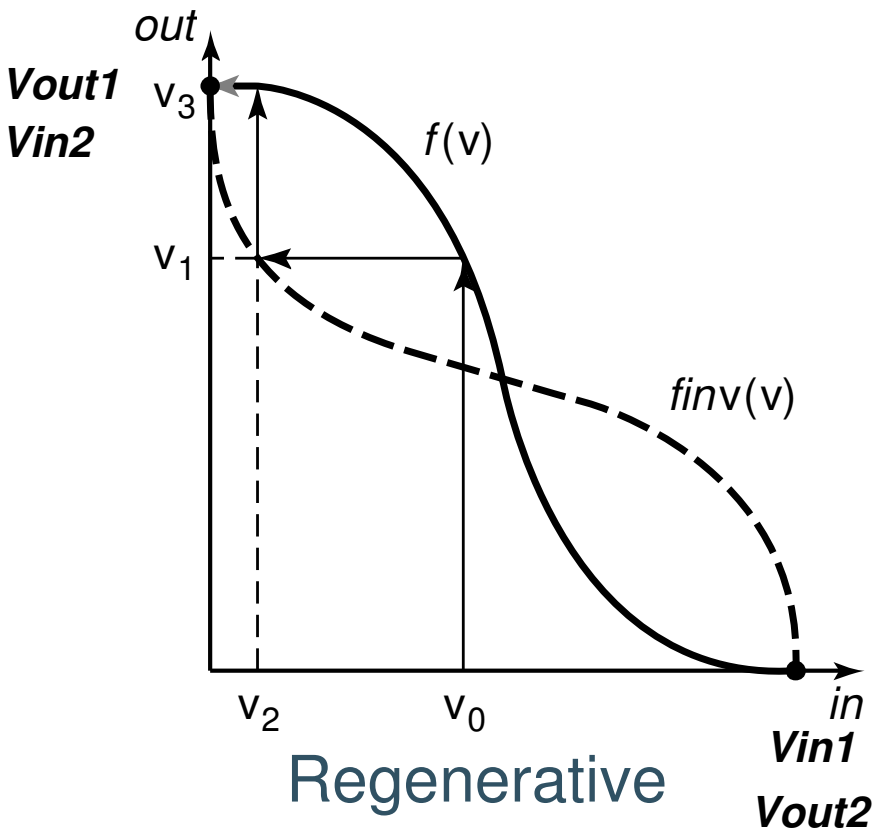


Definition of Noise Margins

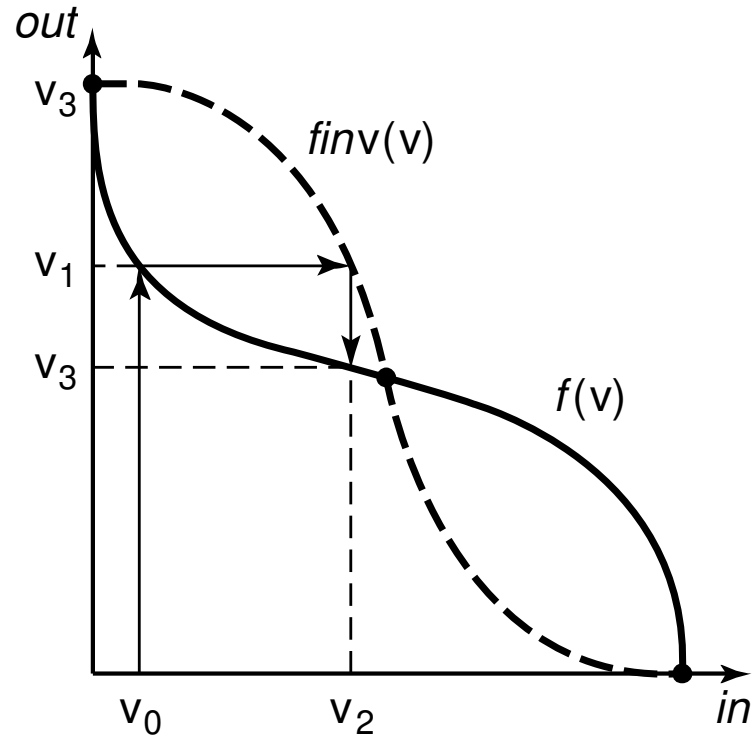


Regenerative Property



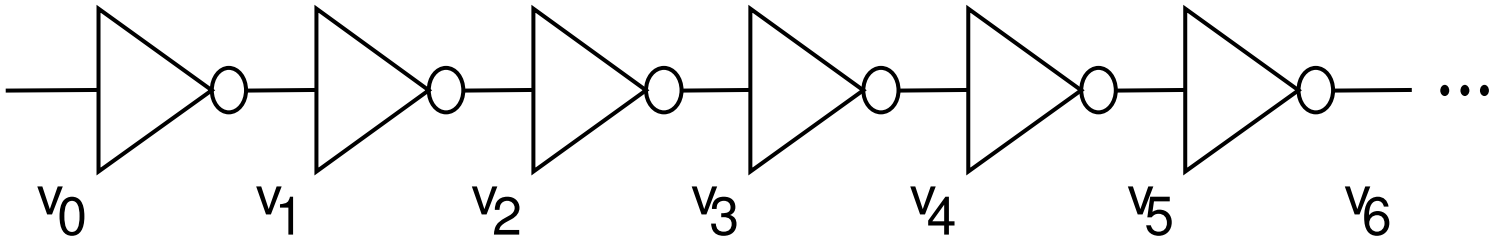


Regenerative

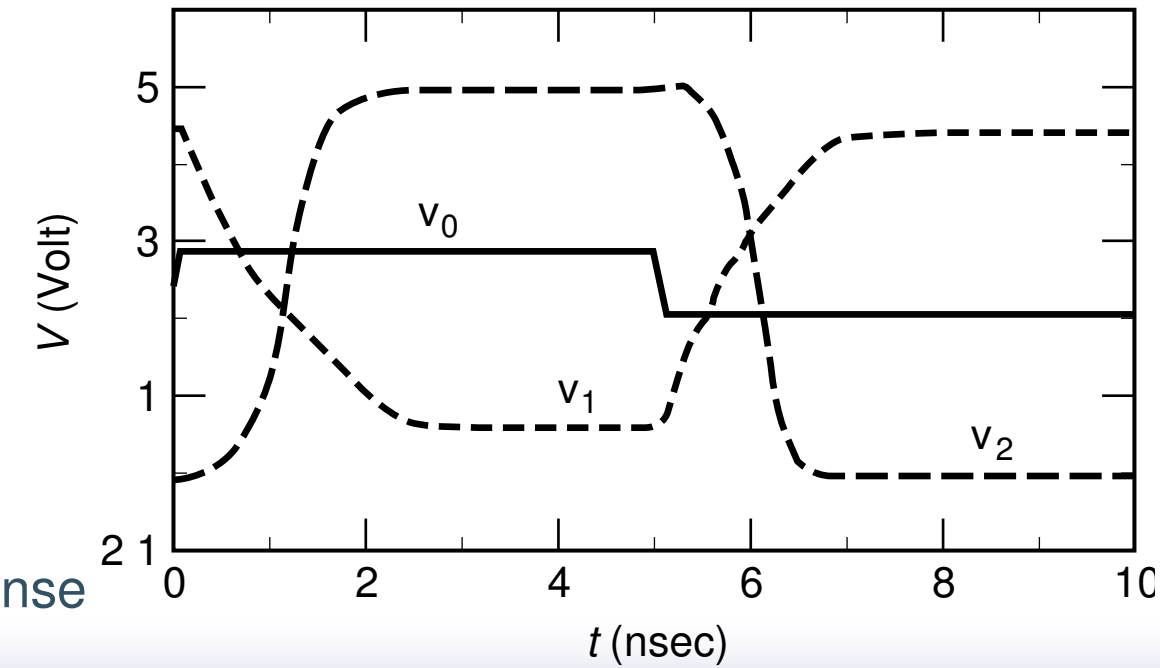


Non-Regenerative

Regenerative Property



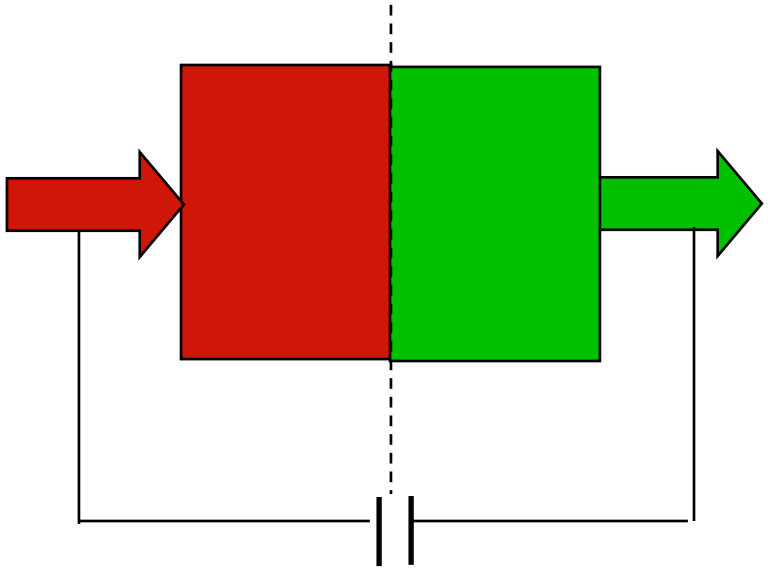
A chain of inverters



Simulated response

Direzionalità

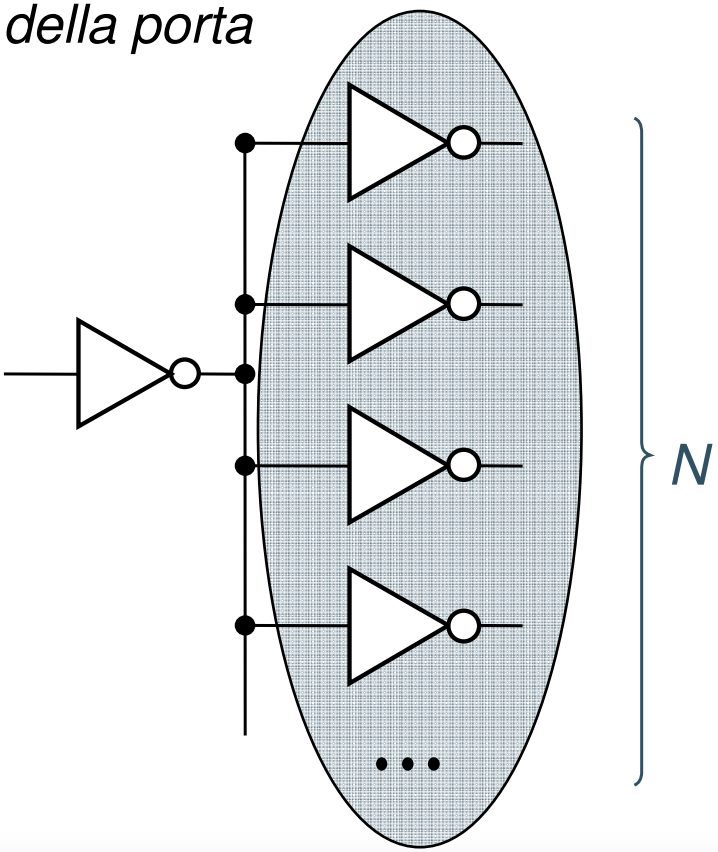
Variazioni sui livelli di tensione in ingresso non devono influenzare i livelli di tensione in uscita



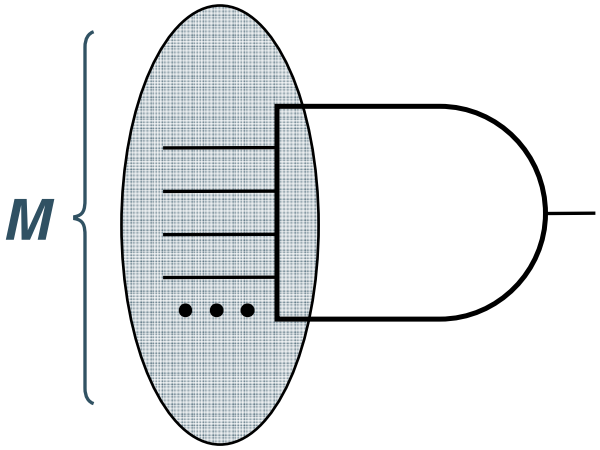
Fan-in and Fan-out

Aumentare il fan-out comporta una variazione del valore logico di tensione e deteriora il comportamento dinamico della porta

La complessità (# transistori) è proporzionale al fan-in

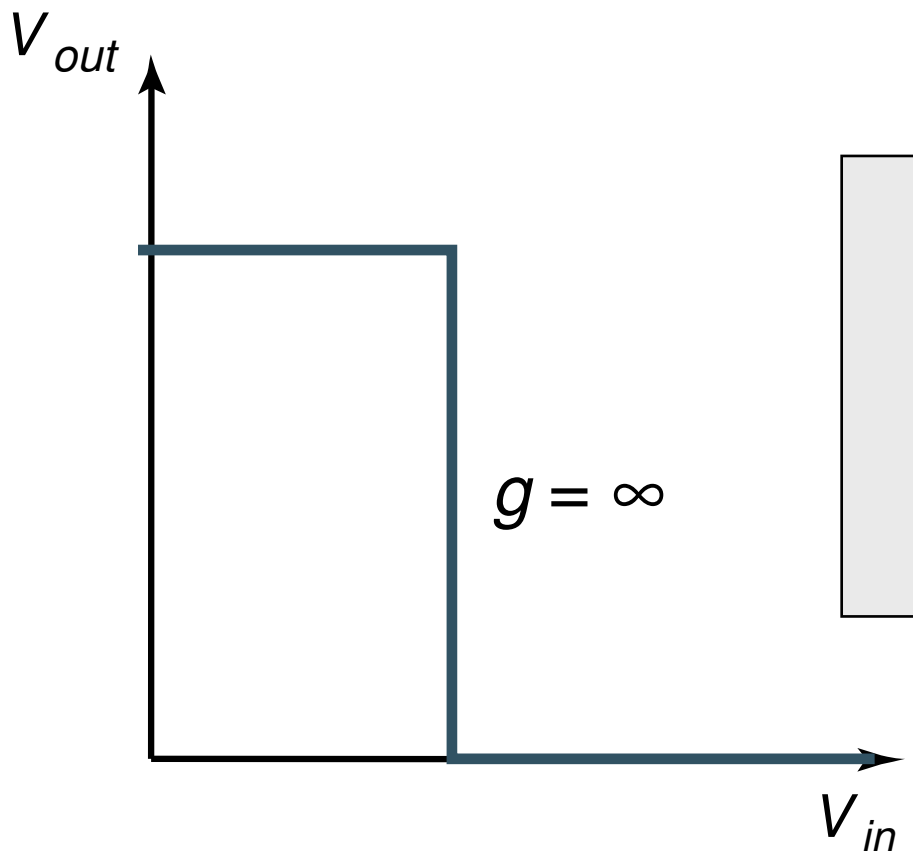


Fan-out *N*



Fan-in *M*

The Ideal Gate



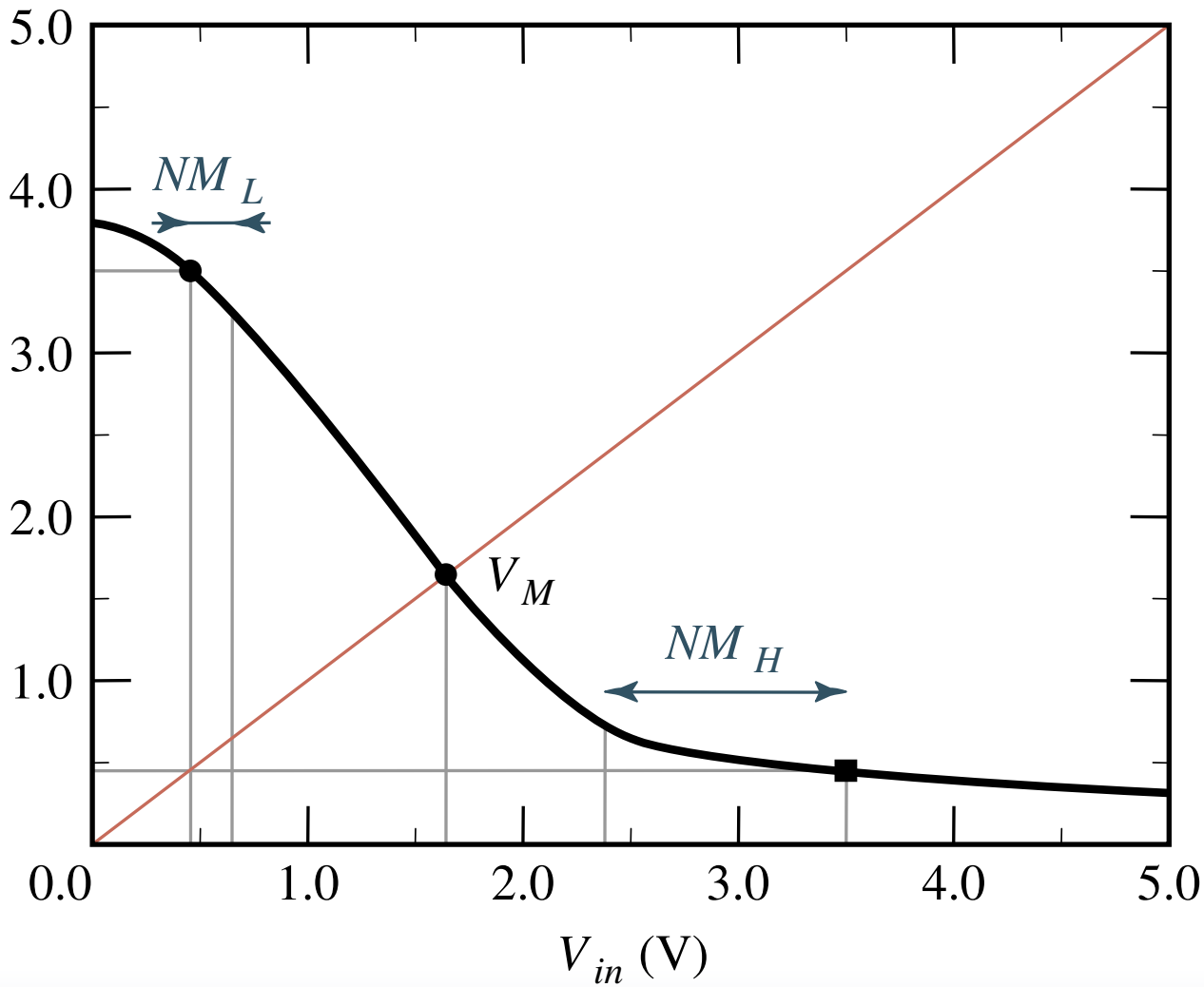
$R_i = \infty$

$R_o = 0$

Fanout $= \infty$

$NM_H = NM_L = V_{DD}/2$

An Old-time Inverter

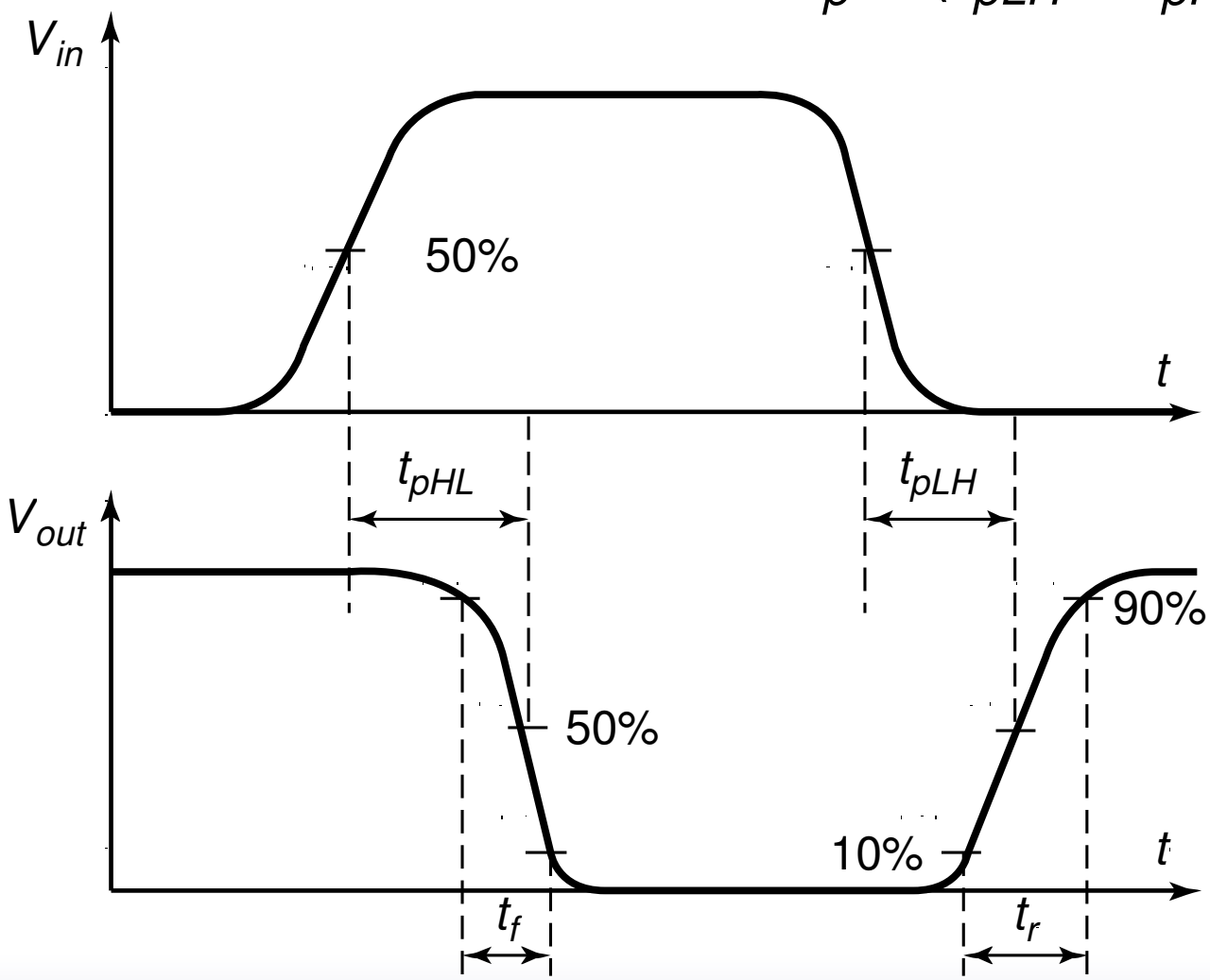


Prestazioni

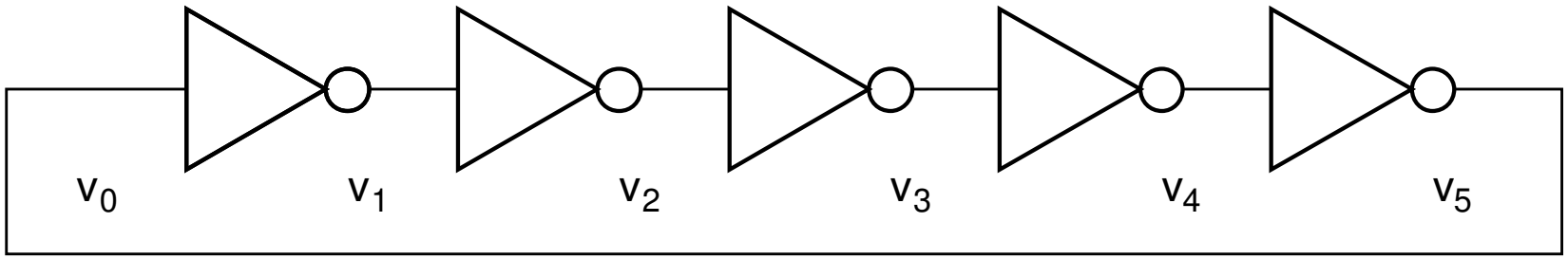
- #operazioni/sec (Architettura)
- Frequenza di clock (Circuito)
- Tempi di propagazione (Porta)

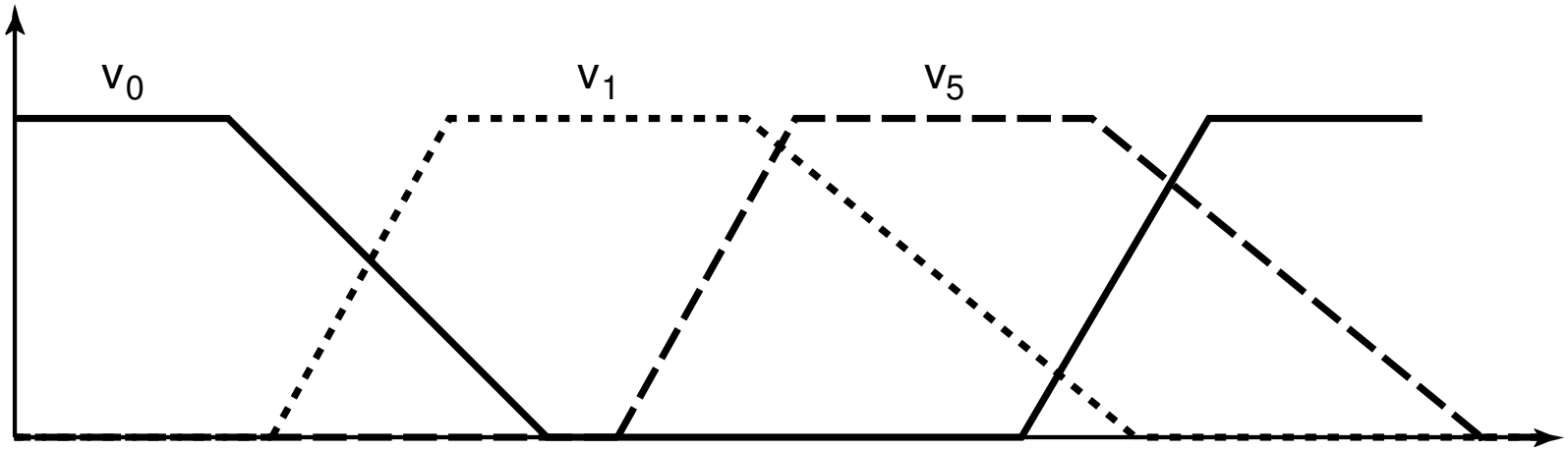
Delay Definitions

$$t_p = (t_{pLH} + t_{pHL})/2$$



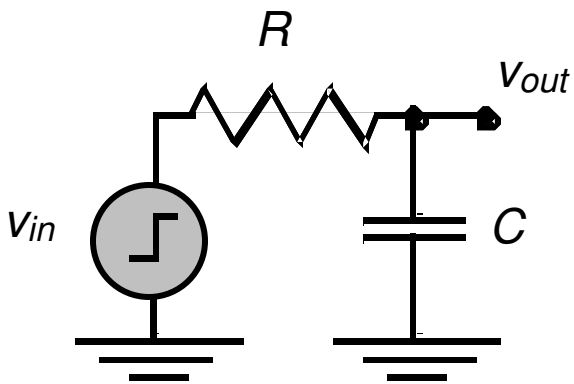
Ring Oscillator





$$T = 2 \times t_p \times N$$

A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

$t_p = \ln(2)\,\tau = 0.69\ RC$
$t_r = \ln(9)\ t = 2.2\ RC$

Important model – matches delay of inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

Energy and Energy-Delay

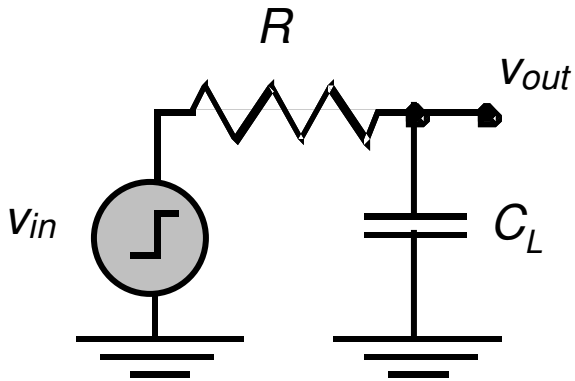
Power-Delay Product (PDP) =

E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

A First-Order RC Network



$$E_{0\rightarrow 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this book
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation