ModelSim XE III Tutorial

This is a brief tutorial on how to run the ModelSim VHDL editor and the ModelSim waveform generator.

Creating a place to save your work

First in "My Documents" create a folder named "ES4" Within this folder create one called "Labs"

Setting Up ModelSim

Before starting, check to see if ModelSim has been registered. Click "Start" to "All Programs" to "ModelSim XE III 6.0a" to "ModelSim" If the program starts up, then no registration is needed. If the ModelSim flashes but the program does not start, then then ModelSim needs to be registerd.

Regsitering ModelSim

Click "Start" to "All Programs" to "ModelSim XE III 6.0a" to "Licensing Wizard" Click "Continue" On the following screen, click "Browse" and navigate to or type in "C:\Modeltech_xe_starter\license.dat" or "C:\Modeltech_xe_starter\win32xoem\license.dat" Click Continue and let the program register itself

Now start the ModelSim Project Navigator

Click "Start" to "All Programs" to "ModelSim" to "Project Navigator" You should get a screen similiar to the following



Creating a Project

Click on "File" and then "New Project"

In the "Project Location:" point it ot where your folder has been created

Then enter a project name.

M Create Project 🛛 🔀
Project Name
Project Location
nts and Settings/sveera03/Desktop Browse
Default Library Name
work
Copy Settings From
ech_xe_starter/modelsim.ini Browse
Copy Library Mappings C Reference Library Mappings

Click "OK" and select "Create a New File" from the pop-up menu.



Type the file name for example "andgate" and select the file type as VHDL. This will create a file name andgate.vhdl which is visible in the work space window.

Editing VHDL

Now, double click on the link 'andgate.vhdl" in the work space window to invoke the vhdl editor that you can type in your program.

ModelSim XE III/Starter 6.3c - Custom Xilin	Version	
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Name Statu: Type Orde: Modifier	ln #	_
andgate.vhd VHDL 0 02/11/0	3 use IEEE.STD LOGIC ARITH.ALL;	
	4 use IEEE.STD_LOGIC_UNSIGNED.ALL;	
	5	
	6 entity and_gate is	
	/ port (a: in std_logic;	
	9 c: out std logic):	
	10 end and gate;	
	11	
	12 architecture Structural of and_gate is	
	13 begin	
	14 $c \le a$ and b;	
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	17	_
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📸 Project 🏨 Library 🖆	B H andgate.vhd	()
Transcript		26 H :
# Loading project Es4		-
<pre># reading C:\Modeltech_xe_starter\win32xoem//models # Loading project firstlab</pre>	lini	
· · · ·		
ModelSim>		
Transcript		<u> </u>
Project : firstlab <no design="" loaded=""></no>		Ln: 1 Col: 0

Enter in the VHDL code between the "begin" and "end" of the structural and the and gate will be done

```
🛯 and_gate.vhd
    library IEEE;
 1
 2
    use IEEE.STD LOGIC 1164.ALL;
    use IEEE.STD LOGIC ARITH.ALL;
 з
 4
    use IEEE.STD_LOGIC_UNSIGNED.ALL;
 5
 6
        Uncomment the following lines to use the declarations that are
    ---
 7
    ___
         provided for instantiating Xilinx primitive components.
 8
    --library UNISIM;
 9
    --use UNISIM.VComponents.all;
10
11
    entity and gate is
12
        Port ( a : in std logic;
13
                b : in std logic;
14
                c : out std logic);
15
    end and gate;
16
17
    architecture Structural of and gate is
18
19
    begin
20
         c \ll a and b;
21
    end Structural;
22
< 111
```

After editing the code, save the file (Ctrl+S)

Compilation

Click on Compile in the Tool bar and select Compile All. The message appearing should say

Compile of andgate.vhd was successful.

Simulation

To start the simulation click on the Simulation menu from the Tool bar and select "Start Simulation". And enter the name of the entity from your code in the pop-up menu, in this case "andgate".

Ī	A Start	Simulation			X
	Design	VHDL Verilog	Libraries) S	5DF Others	< »
	Name		Туре	Path	
	⊡- ∭	work	Library	C:/Documents and Settings/sveera03/	
	⊡ili	aim	Library	\$MODEL_TECH//xilinx/vhdl/aim	
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	⊡ili	pls	Library	\$MODEL_TECH//xilinx/vhdl/pls	
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The next window should appear

ModelSim XE III/Starter 6.3c - Custom Xilinx Version								
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Workspace		K Objects	🛨 🖻 🗶 📊 C:/Documents ar	nd Settings/sveera03/Desktop/work/andgate1.vhd	부 립 ×			
▼ Instance	Design unit Design unit type	v Value	BP ln #		<u>_</u>			
andgate1	andgate1(s Architecture	a 🍫 a 🛛 U	1	librory TEFF.				
-@ line_14	andgate1(s Process	- ? ^b		TIDIALY INDE;				
std_logic_unsigned	std_logic_un Package		2	USO TEEE STD LOCIC ADIMA ALL:				
std_logic_arith	std_logic_arPackage	-		USO TEEE STD LOCIC UNSTONED ALL.				
sta_logic_1164	sto_logic_1 Package	1	5	use iss.sib_hourc_owsigwab.And,				
stanuaru	scaliuaru Package	1	6	entity endgetel is				
			7	port (a: in std logic:				
			, a	b: in std logic;				
			9	g: out std logig):				
			10	end andgatel:				
			11	ona anagaoor,				
			12	architecture Structural of andgatel is	-			
			13	begin	-			
			14	$c \le a$ and b:				
			15	end structural;				
			16					
			17					
			18					
			19					
					<u>_</u>			
				(<u> </u>			
Project 🏨 Library	🔊 sim 📓 Files 📑 Memc 🗐		H andgate1.vhd		<u> </u>			
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# Loading ieee.std_logic_unsig # Loading work.andgate1(stru	gned(body) uctural)				_			
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Project : samand Now: 0 ns 1	Delta: 0 sim:;	/andgate1						

The Objects window will display the signals available

This is where values can be set and signals can be added to the waveform

Objects	+	₫ <u>×</u>
Name	Value	
🧇 а	U	
🧇 Ь	U	
🧇 с	U	

To add a signal, select the signal, right click on the signal "Add to Wave" then "Selected Signals"

The Wave window will be where your data will output to

💶 wave - default	wave - default						
Messages							
<pre>/andgate1/a /andgate1/b /andgate1/c /andgate1/c</pre>	U U U						
L≣ ● Now Dursor 1	0 ns 0 ns	15 0 ns	500) ns			
H andgate1.vhd wave							

Editing in ModelSim

To test the and gate, several parameters will need to be set Select a waveform, and click "Edit" to "Force"

Objects		🖬 wave - default 🛨 🔊	×
Name	Value	Messages	
↔ a ↔ b ↔ c	View Declaration View Memory Contents View Messages Copy Find Insert Breakpoint Add to Wave Add to List Add to List Add to Log	↓ andgate1/a ↓ andgate1/b ↓ andgate1/c ↓ andgate1/c	<u>S</u>
	Add to Dataflow Toggle Coverage		
1		Now 0 ns 500 ns 100 Cursor 1 0 ns 0 ns 100 Image: Solution of the second se	

For signal a set the "Value" to 1 and "Delay for" to 250

Force Selected Signal	×
Signal Name: sim:/and_gate/a	1
Value: 1	
Kind	
Freeze C Drive C Deposit	
Delay For: 250	
Cancel After:	
<u> </u>	

This will set the value of a to be 1 after 250ps

For signal b set the "Value" to 1 and "Delay for" to 500

Force Selected Signal
Signal Name: sim:/and_gate/b
Value: 1
Kind
Freeze C Drive C Deposit
Delay For: 500
Cancel After:
<u> </u>

This will set the value of a to be 1 after 250ps

In the ModelSim window, it shows what the command line execution would be The same thing as above could have been done with signal a by typing "force -freeze sim:/and_gate/a 1 250"

Now type "run 750" in the ModelSim window, which will run the This will run the sytem for 750ps



Analyzing Output

Γ	🔳 wave - default							±₫×
l	Messages							
l	🔶 /andgate1/a	1						
L	/andgate1/b	1						
	 /andgate1/b /andgate1/c 	1						
		750 ns						
	Gursor 1	0.05	0 ps	500	Ins	100	U NS	1500 ns
ŀ	I wave land ate1 wbd]							
1								<u> </u>

The following out is generated by "run 750"

As can be seen, signal a freezes at 1 after a delay of 250ps Signal b freezes at 1 after 500ps

The red line signifies that the data is unknown, which is try since the data is unknown before 250ps and 500ps

Output c is determing function of the two signals throughout the execution, which ends at 750ps