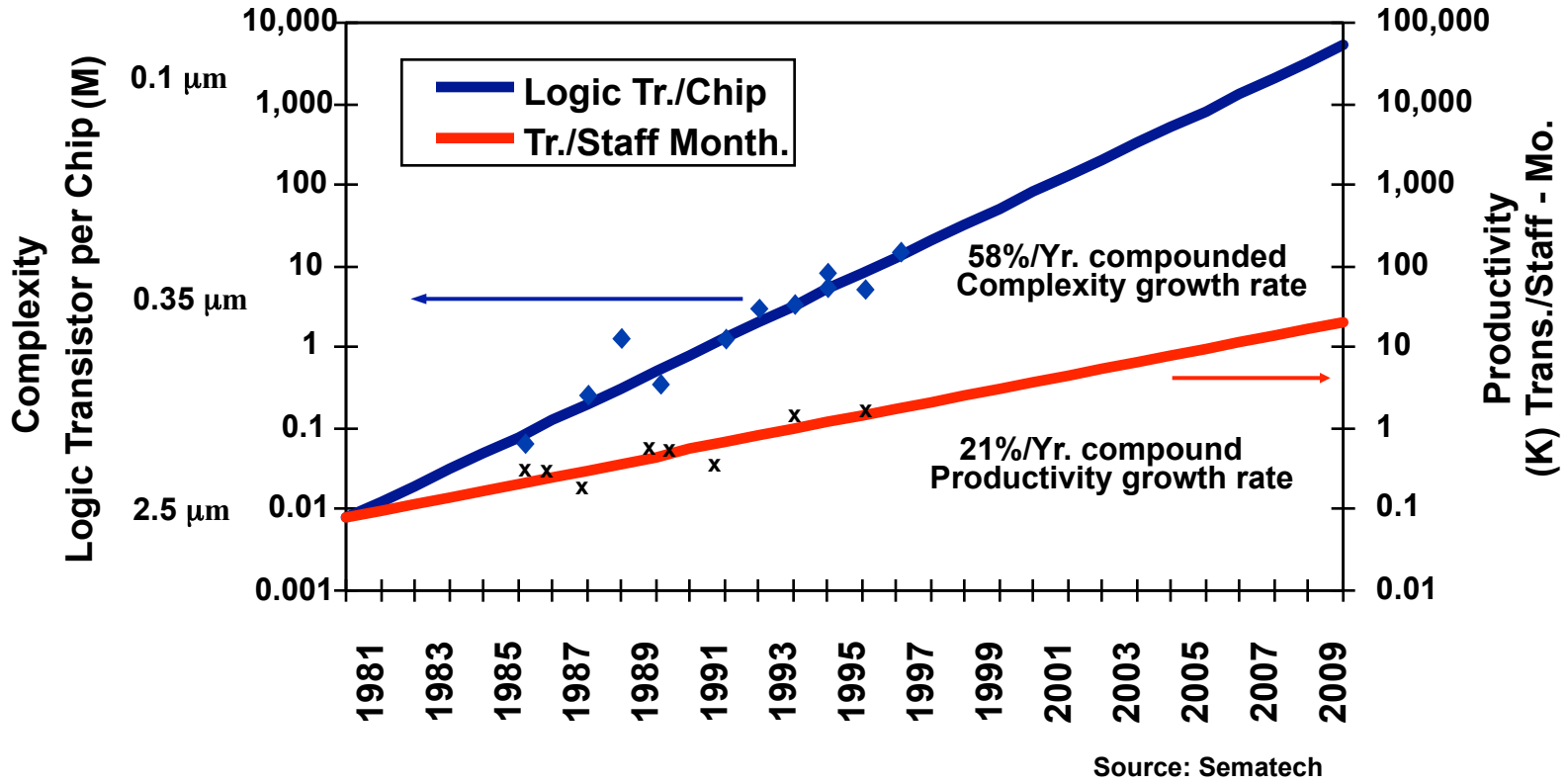
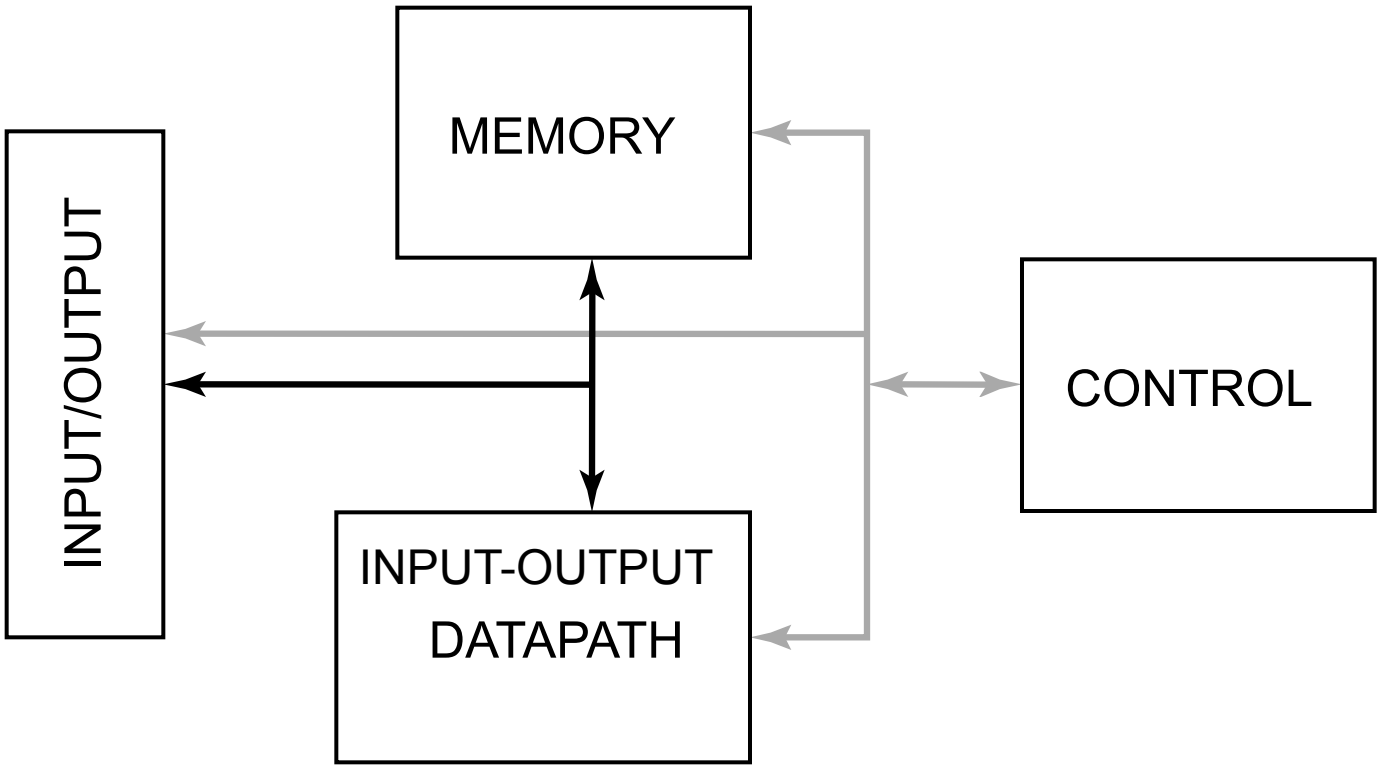
Design Methodologies

Productivity Trends

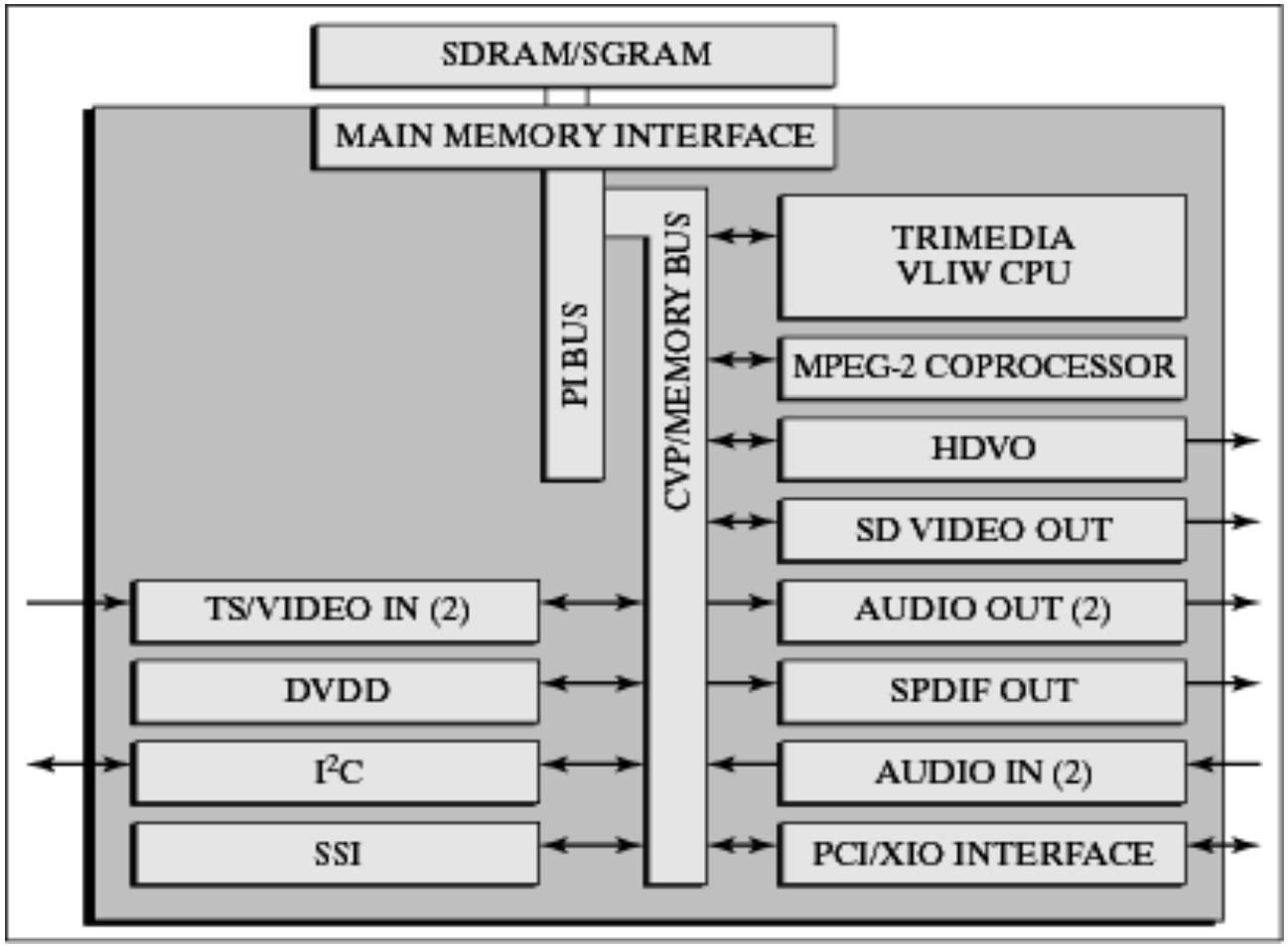


Complexity outpaces design productivity

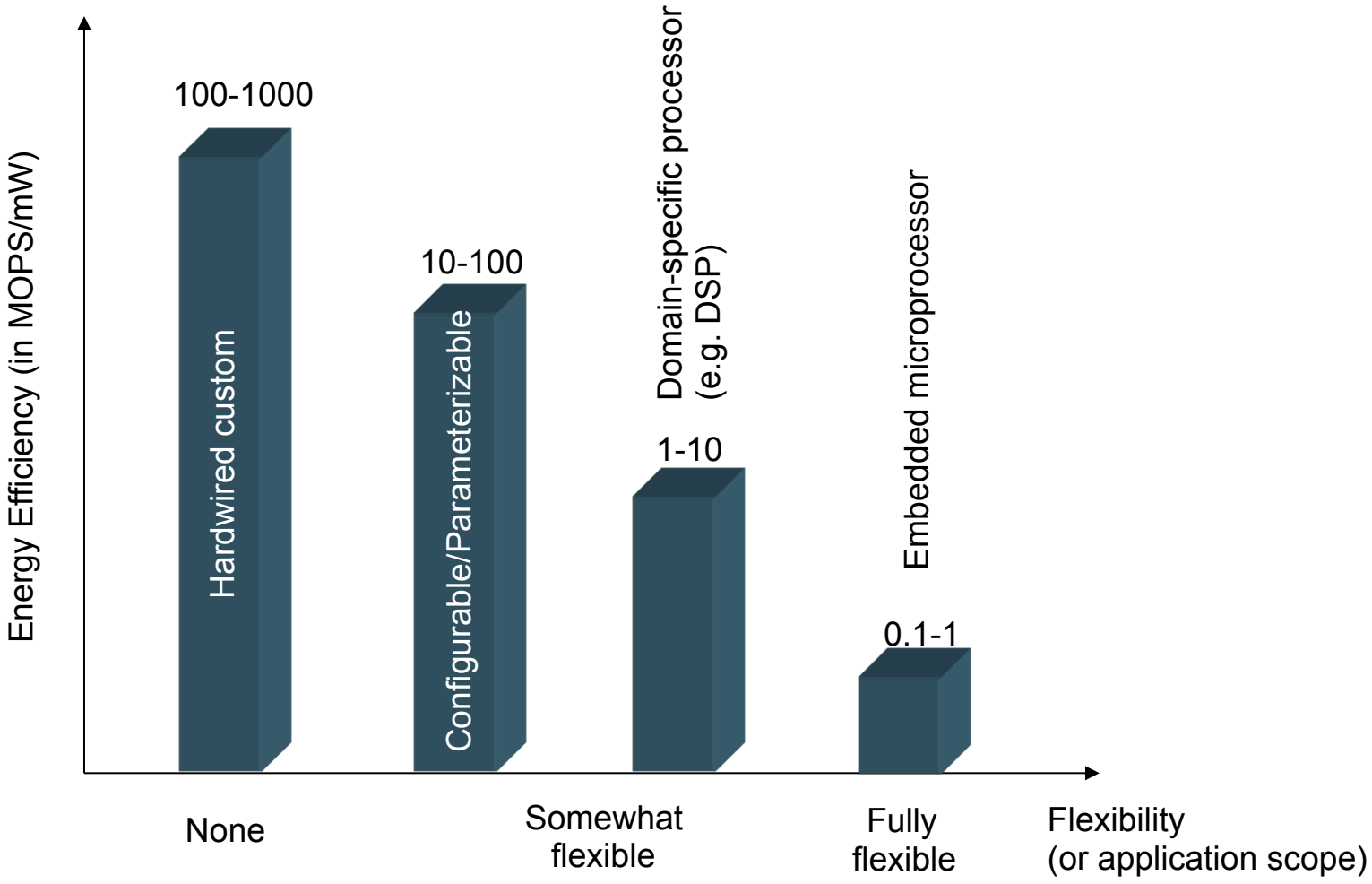
A Simple Processor



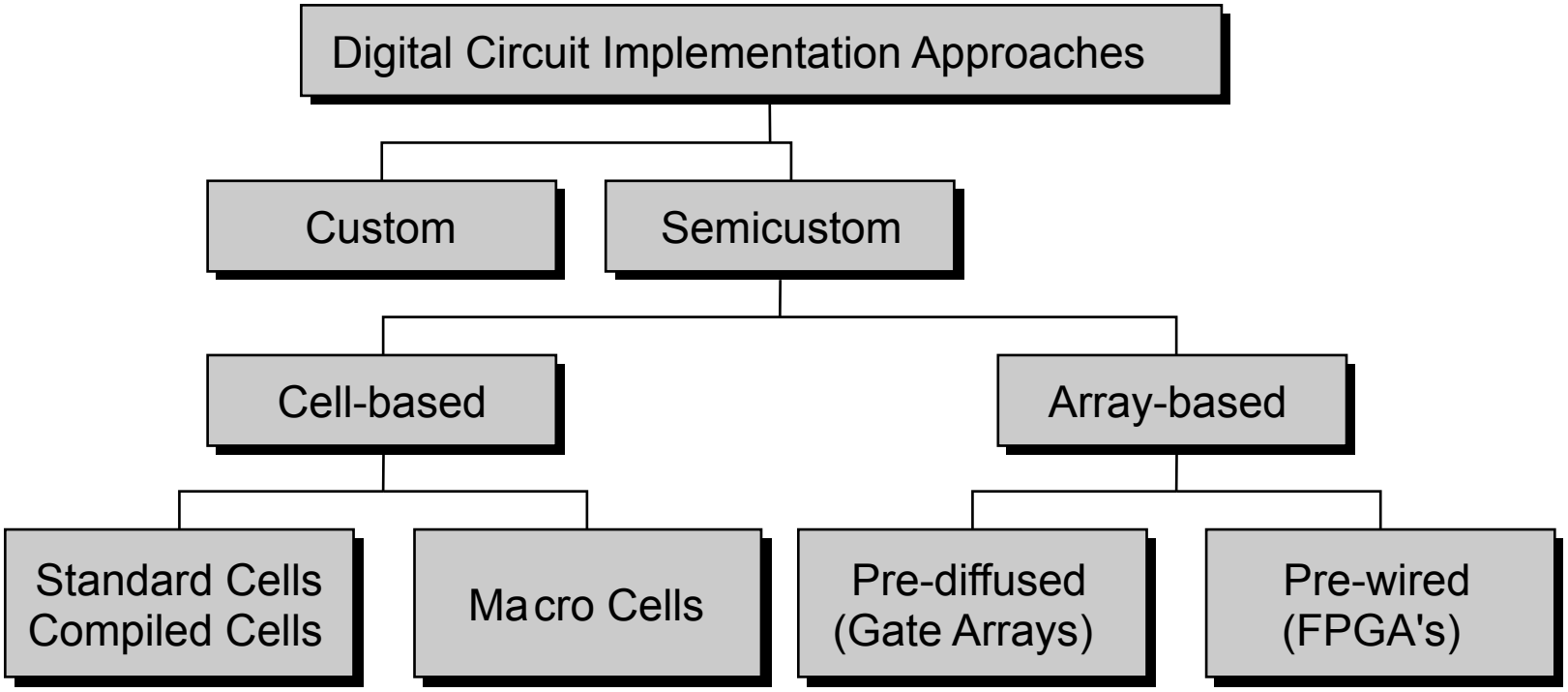
A System-on-a-Chip: Example



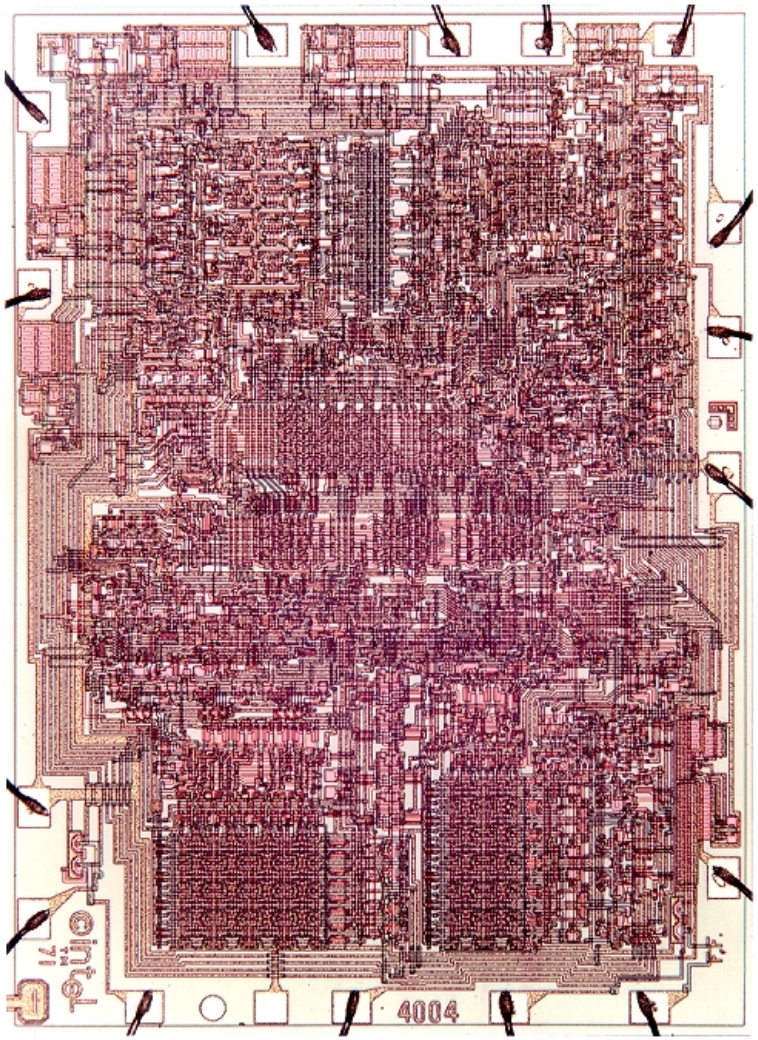
Impact of Implementation Choices



Implementation Choices

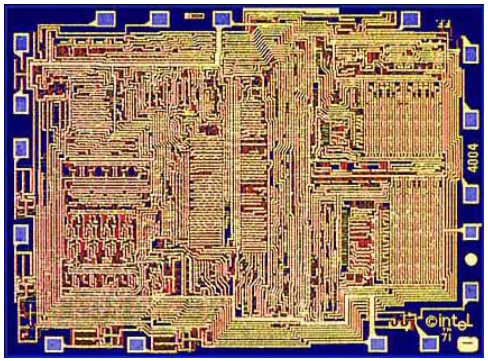


The Custom Approach

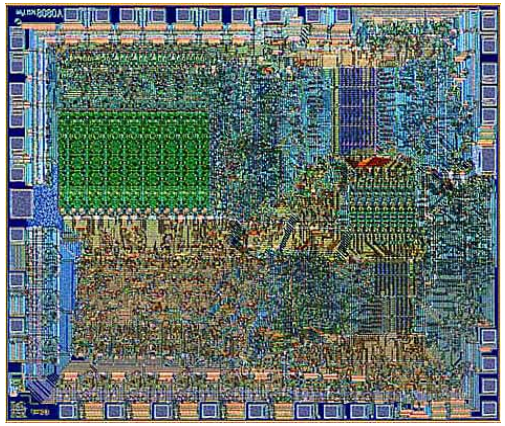


Intel 4004

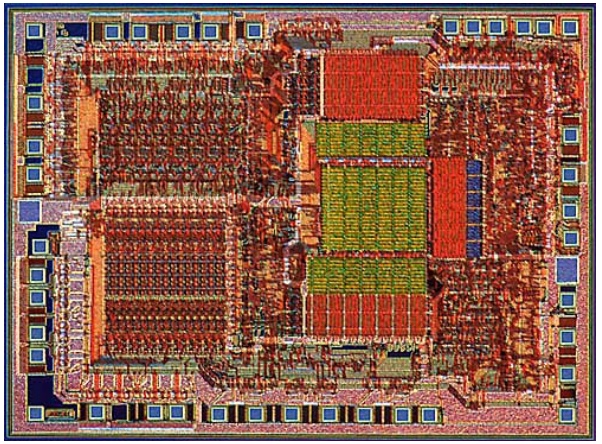
Transition to Automation and Regular Structures



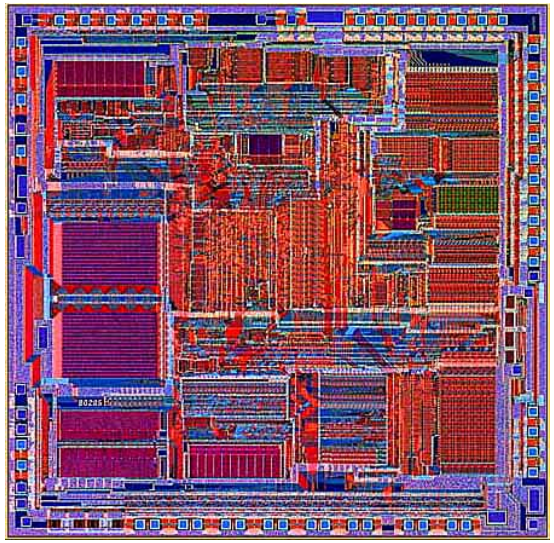
Intel 4004 (‘71)



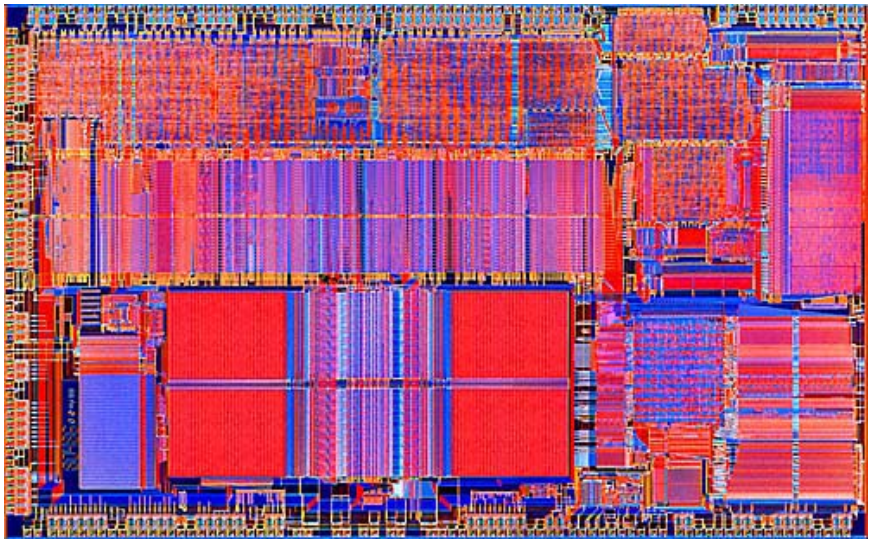
Intel 8080



Intel 8085

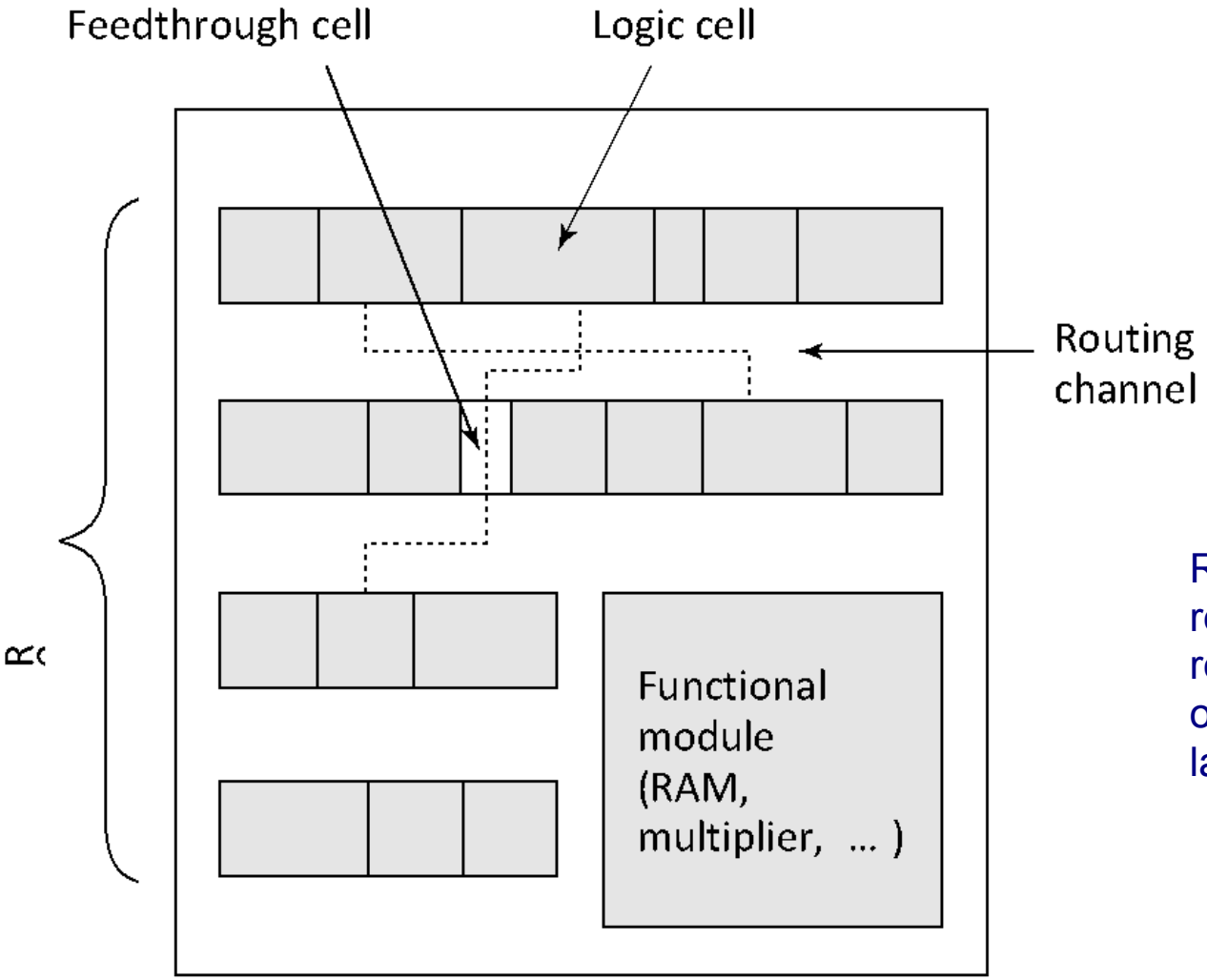


Intel 8286



Intel 8486

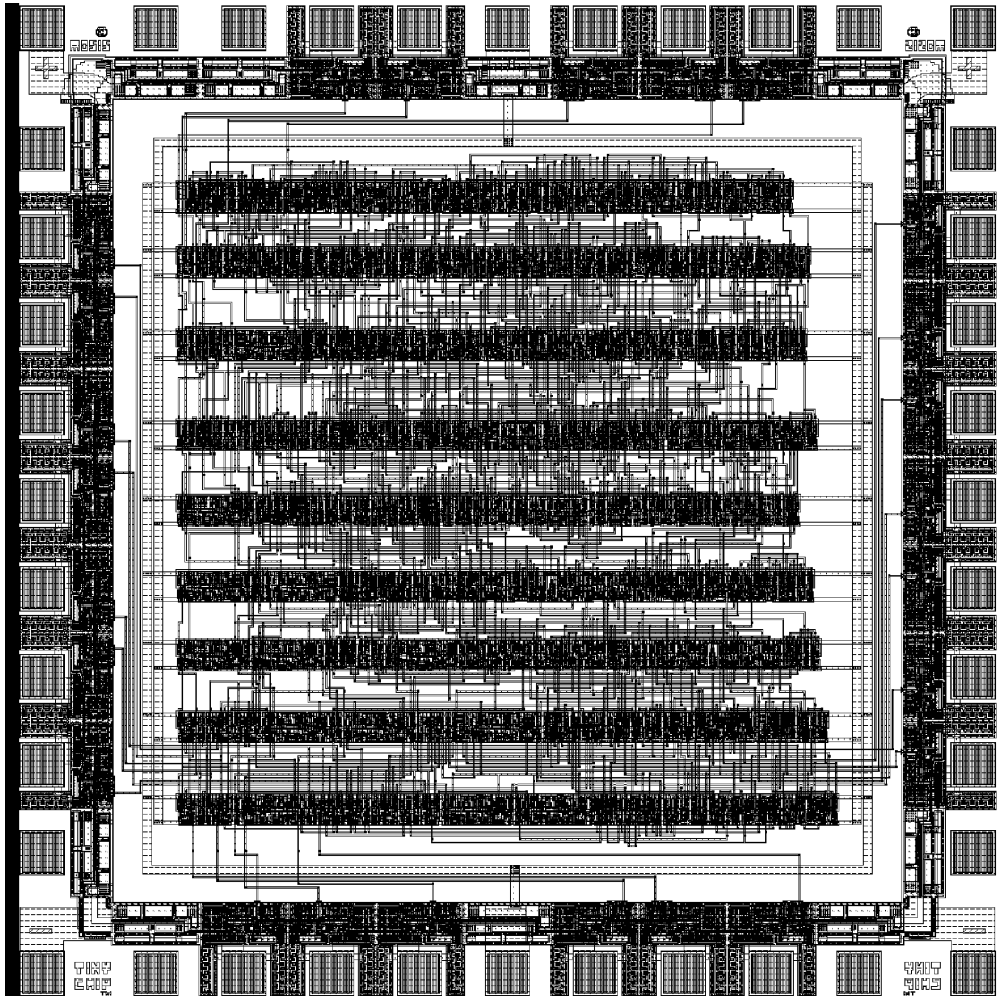
Cell-based Design



Routing channel requirements are reduced by presence of more interconnect layers

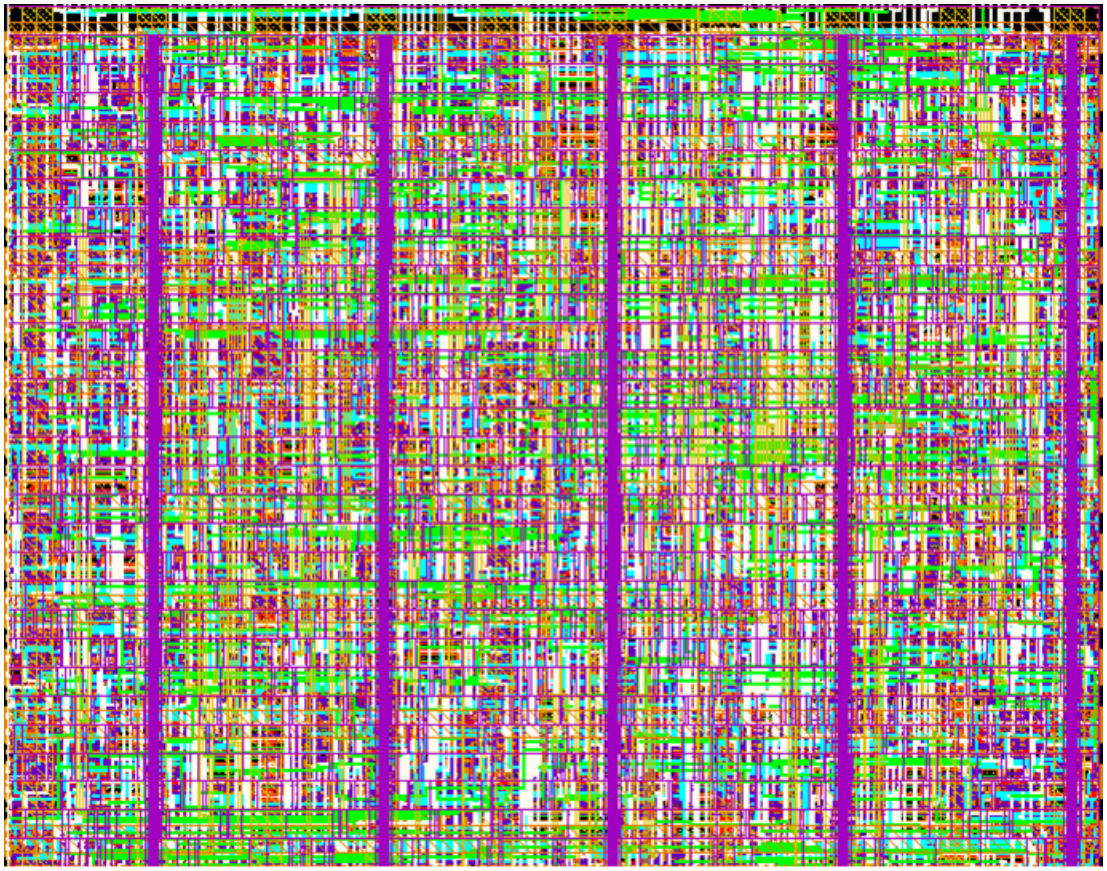
Standard Cell Layout methodology

The Evolution of Standard Cell



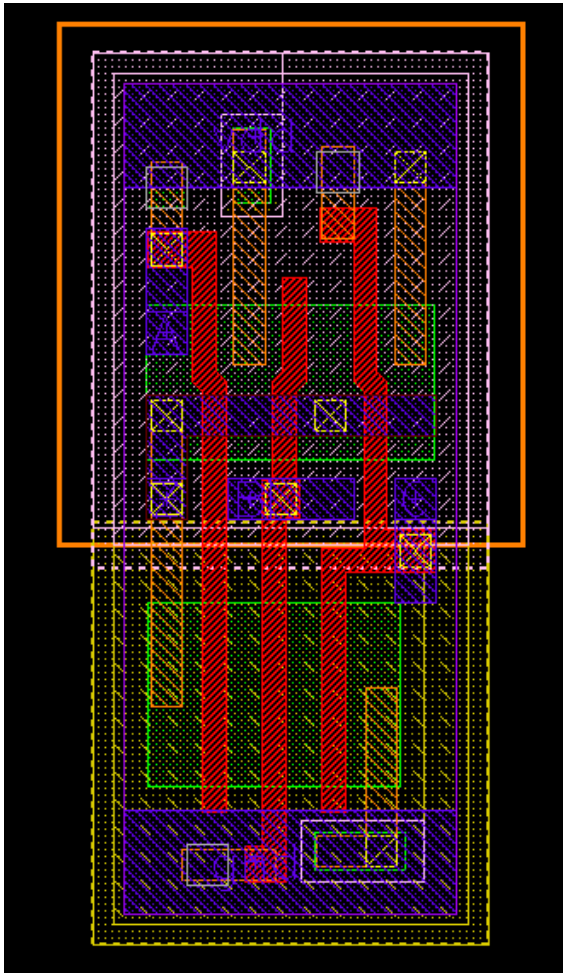
[Brodersen92]

Standard Cell – The New Generation



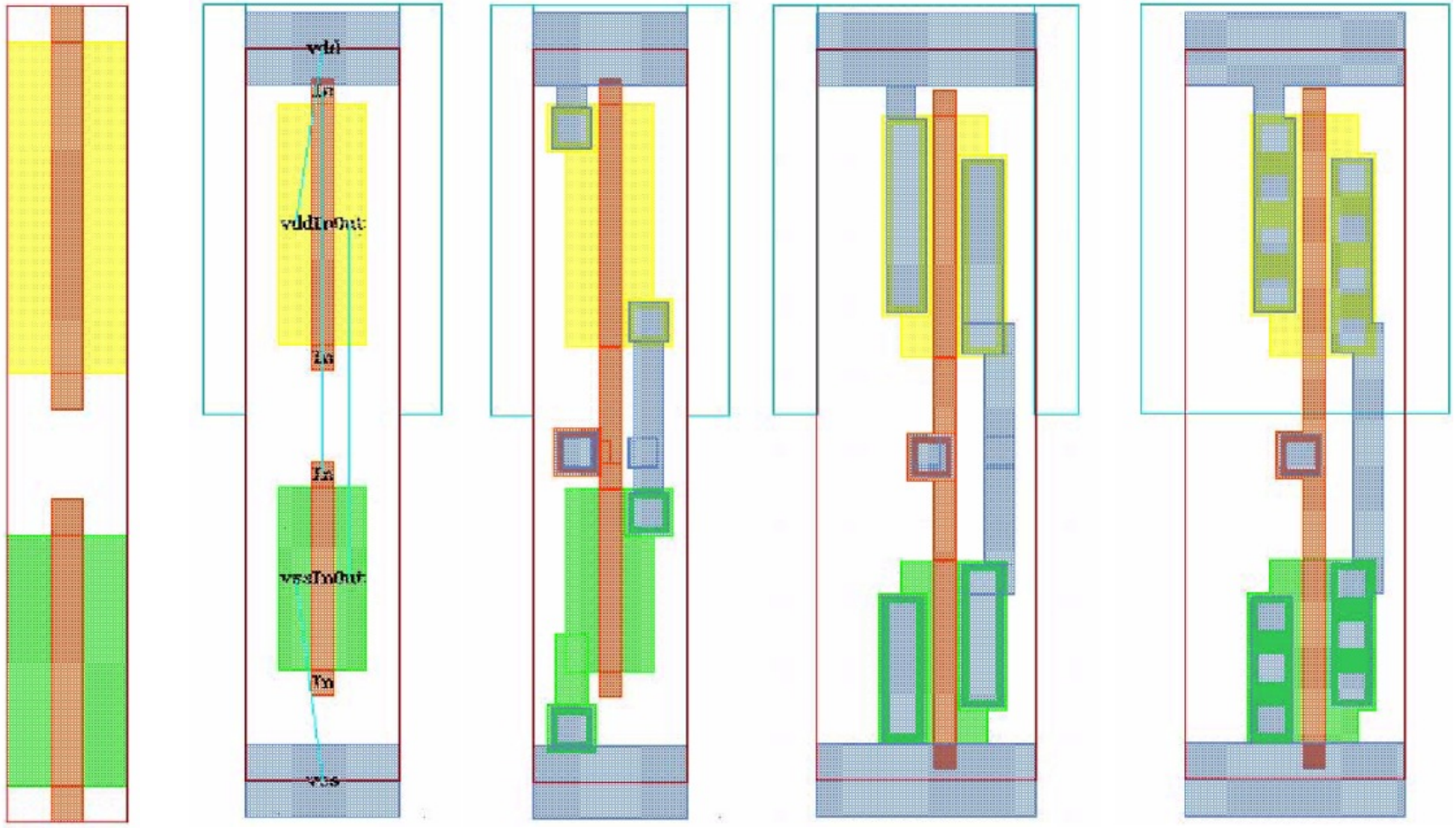
Cell-structure hidden under interconnect layers

Standard Cell - Example



3-input NAND cell
(from ST Microelectronics):

Automatic Cell Generation



Initial transistor geometries

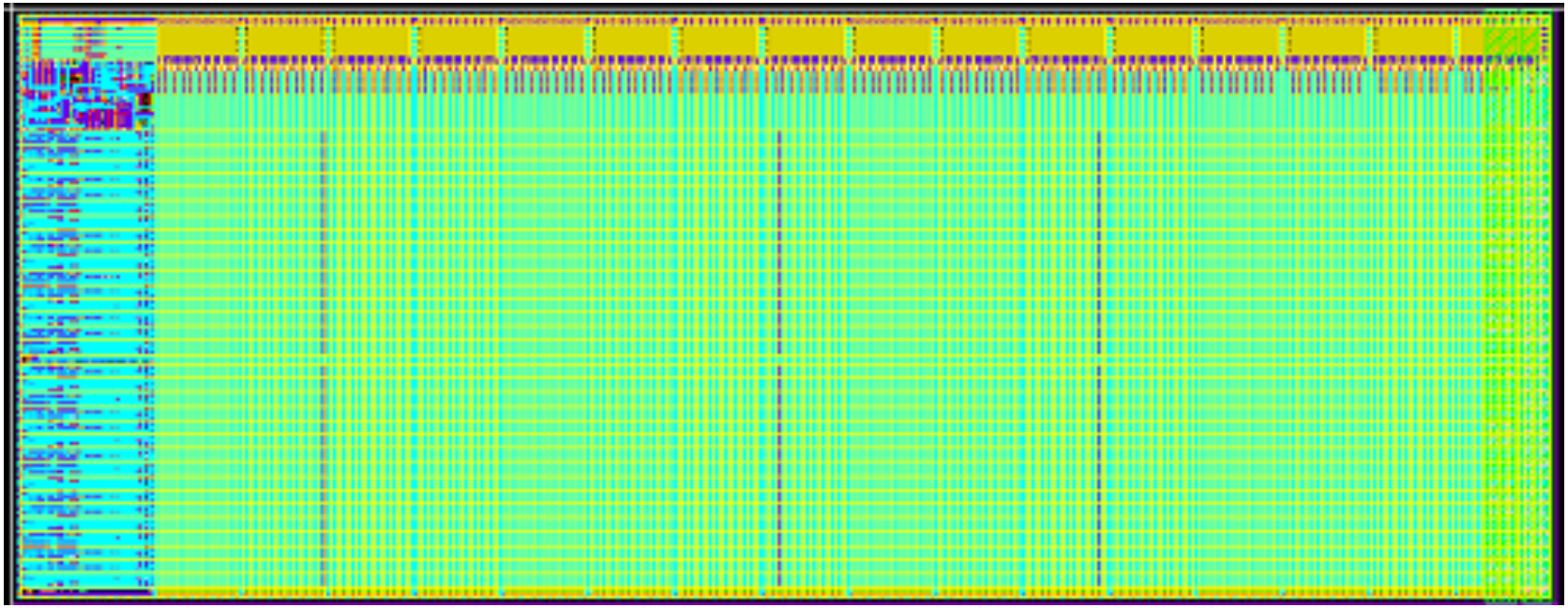
Placed transistors

Routed cell

Compacted cell

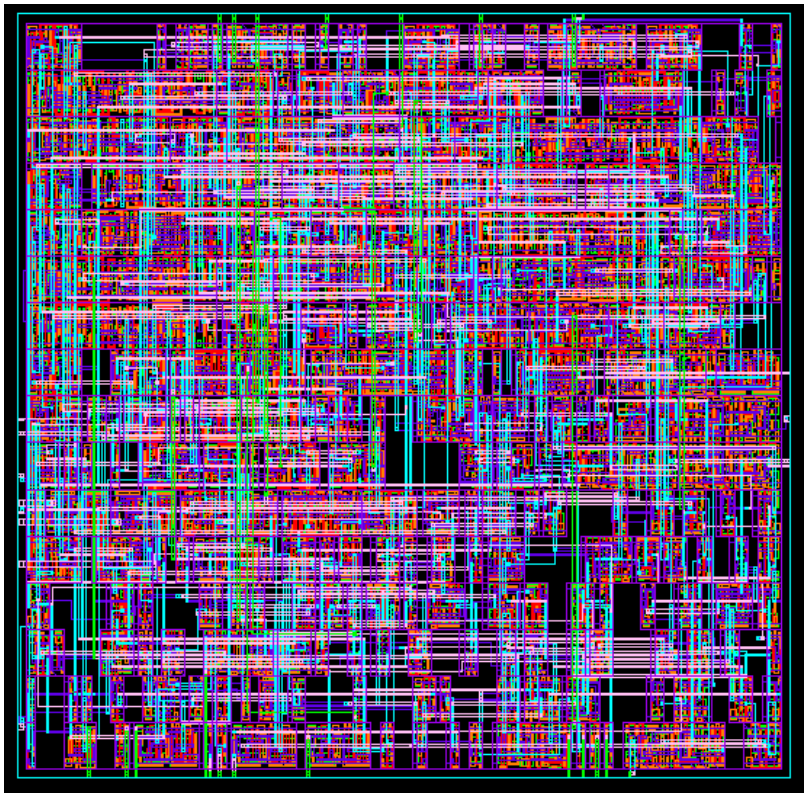
Finished cell

MacroModules

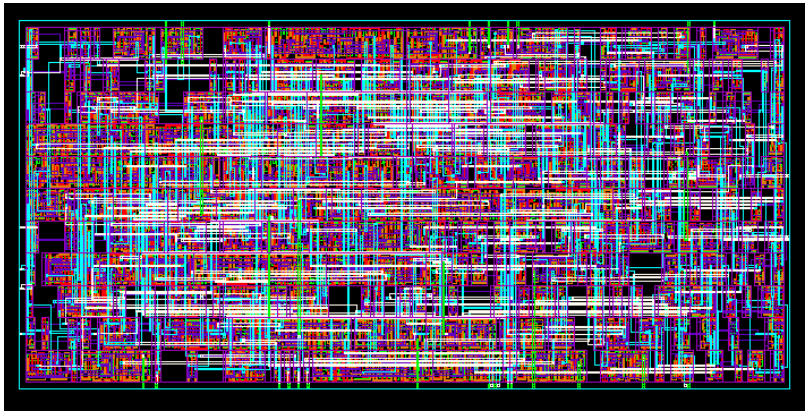


256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator
Implemented in 0.18 μm CMOS technology (0.094 mm^2)

“Soft” MacroModules

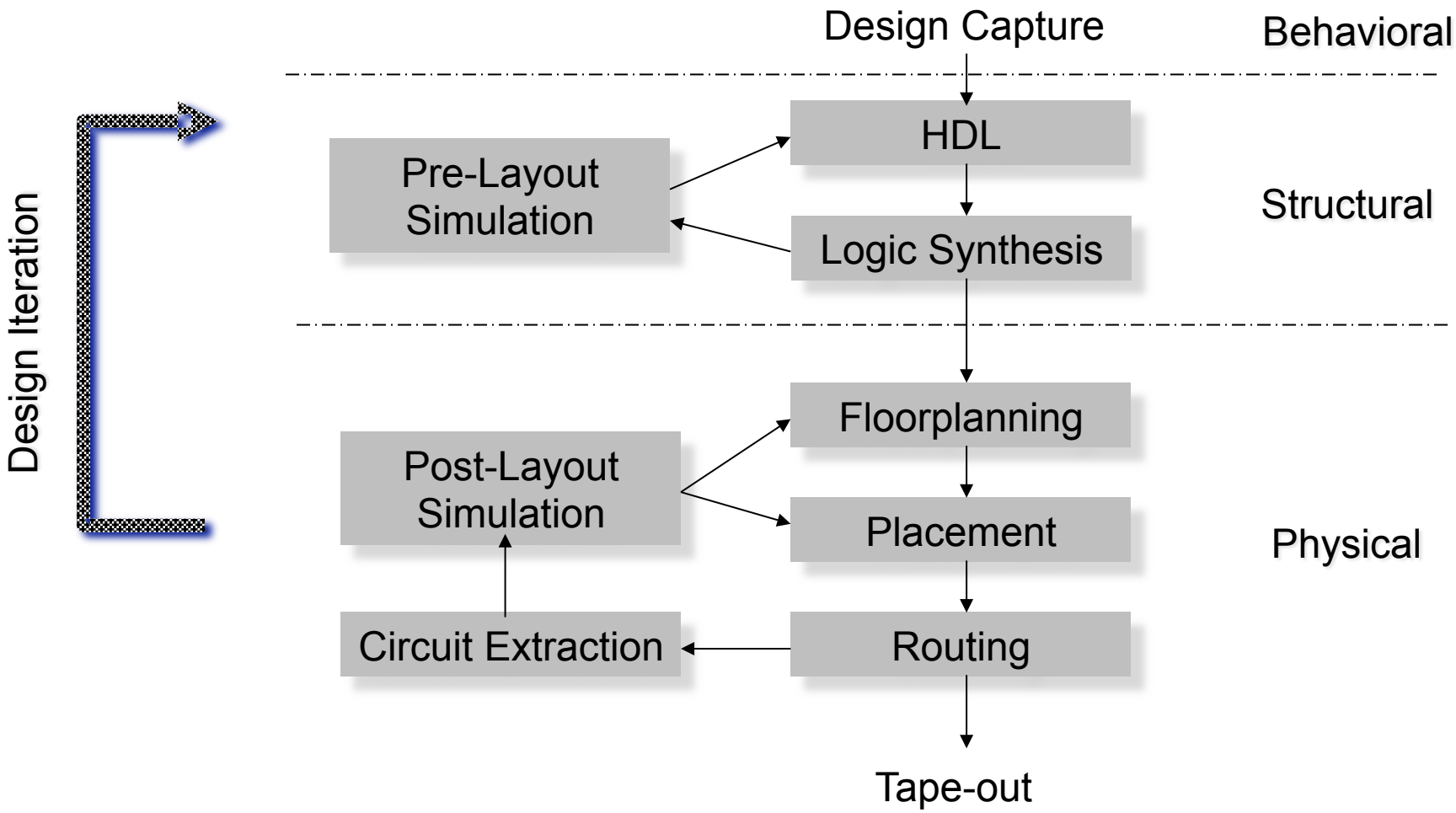


8 x 8 Multiplier

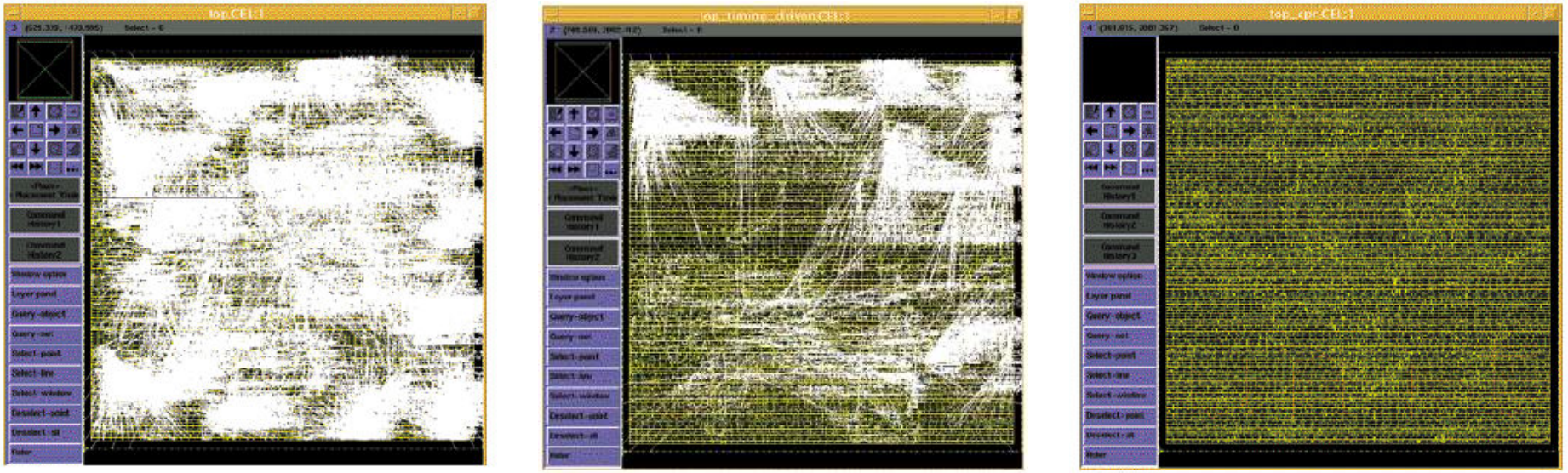


Synopsys DesignCompiler

Semicustom Design Flow



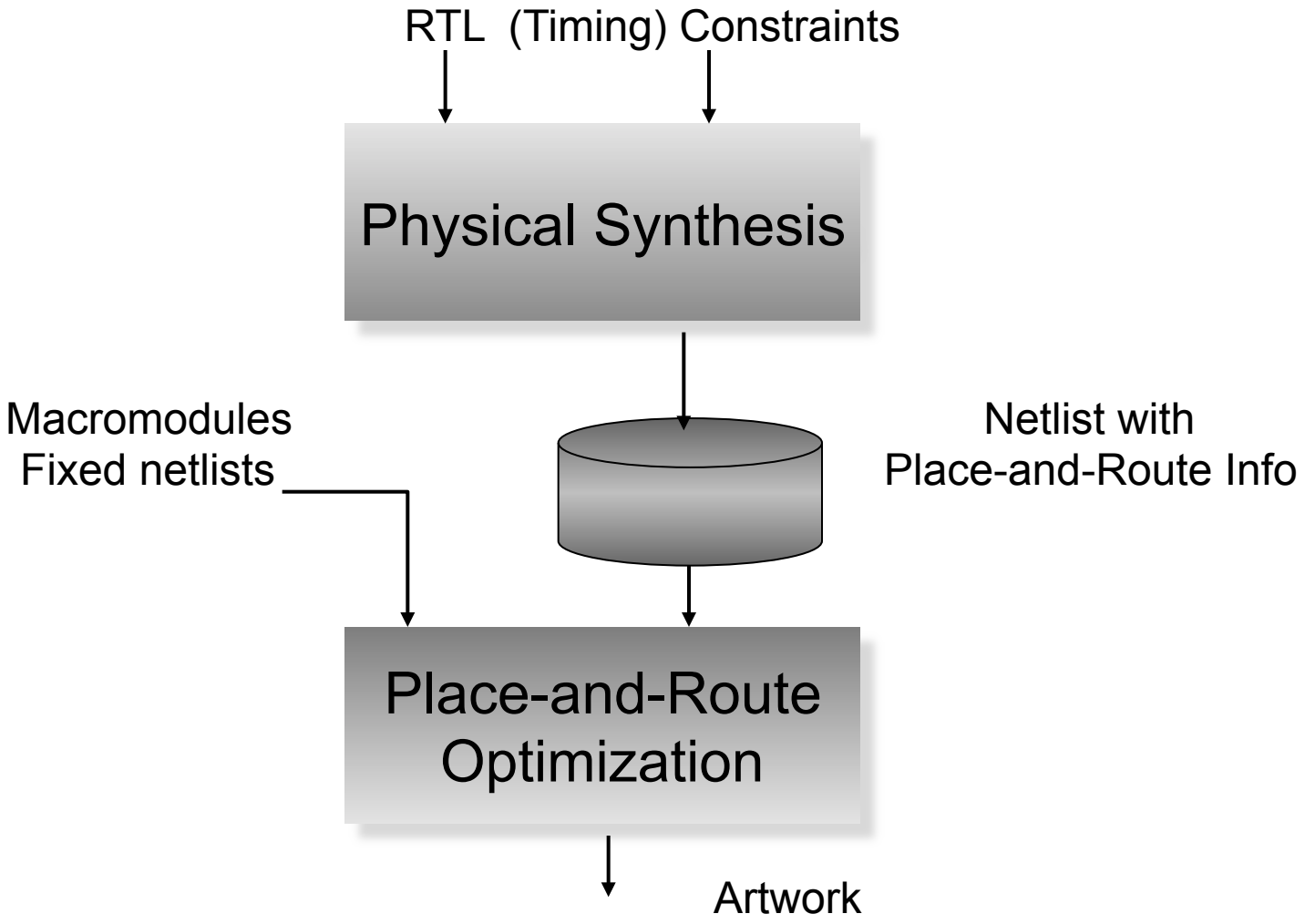
The "Design Closure" Problem



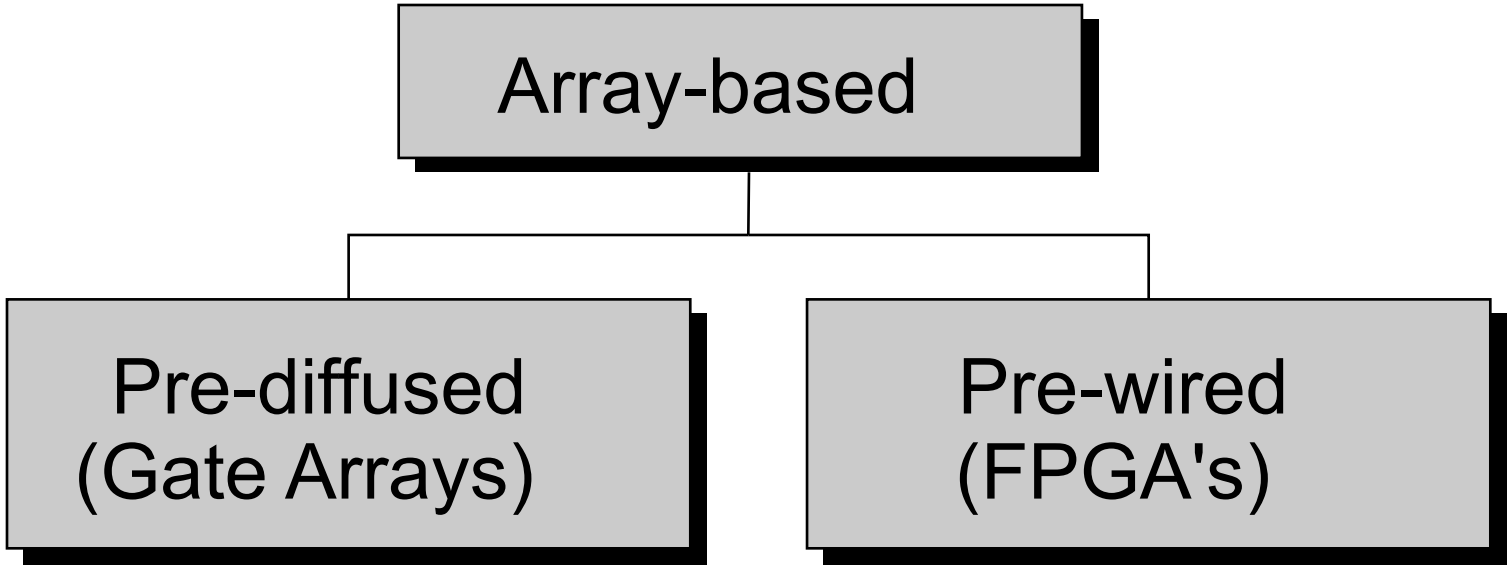
Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

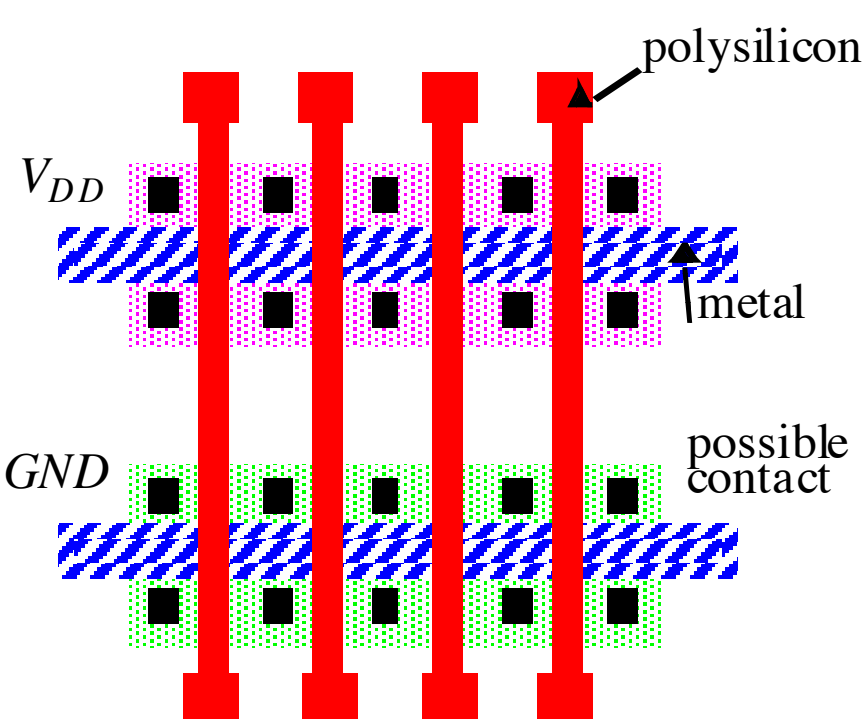
Integrating Synthesis with Physical Design



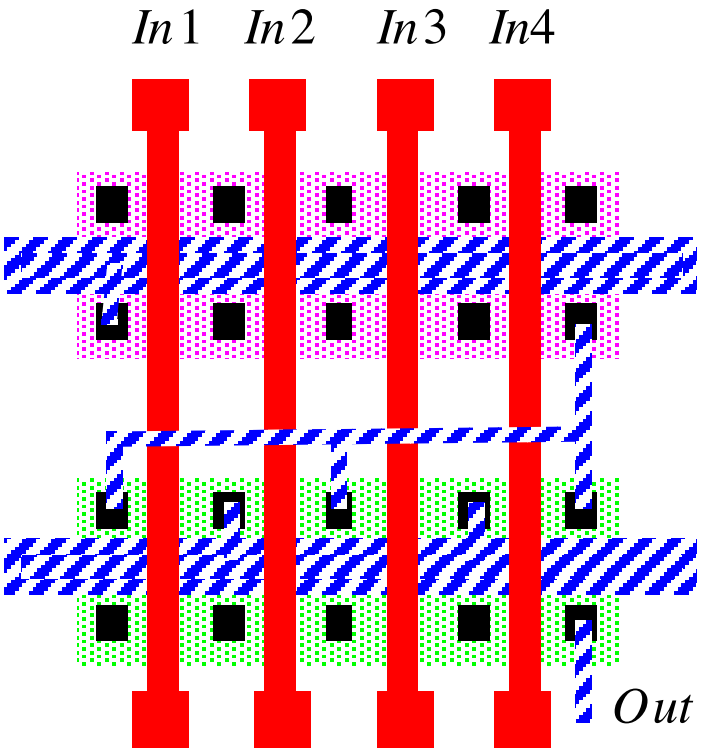
Late-Binding Implementation



Gate Array — Sea-of-gates

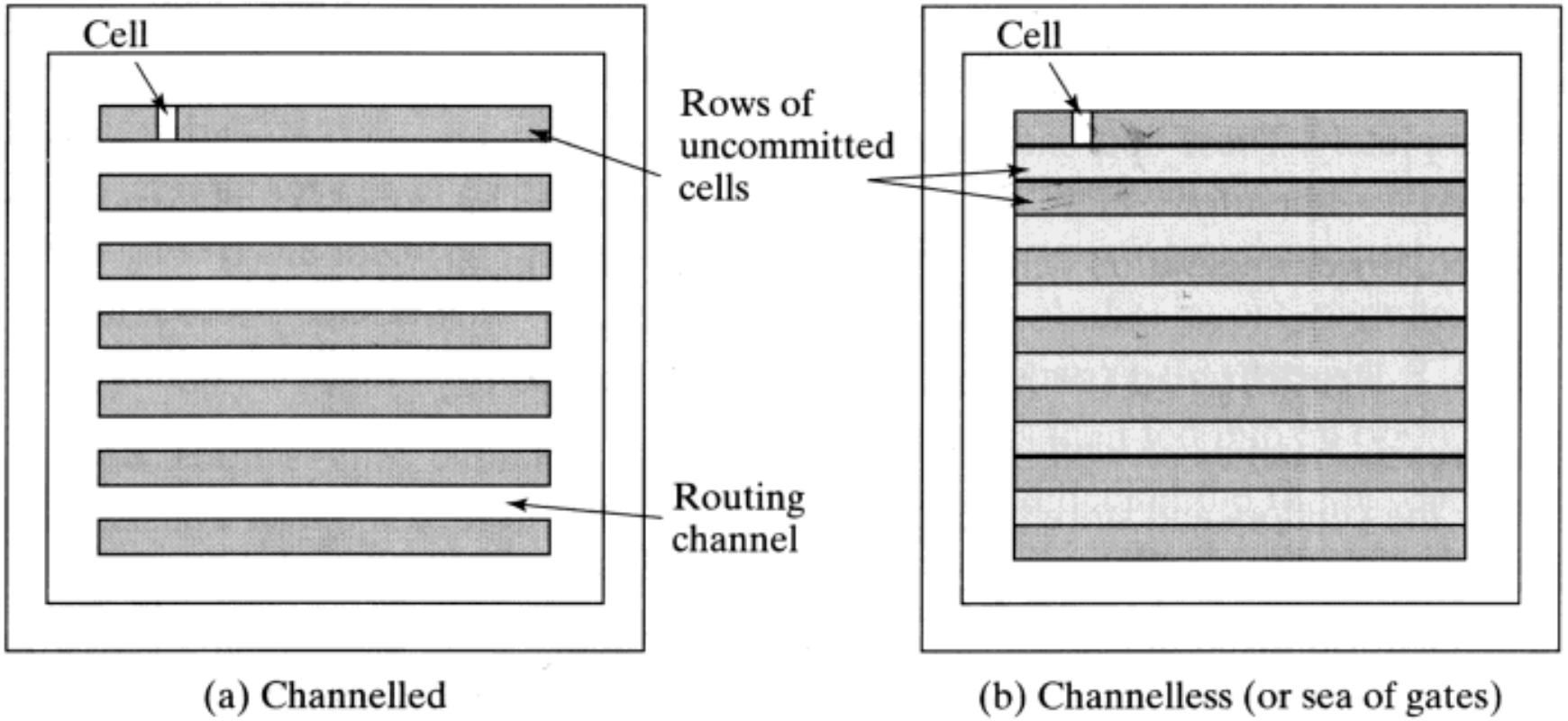


Uncommited
Cell

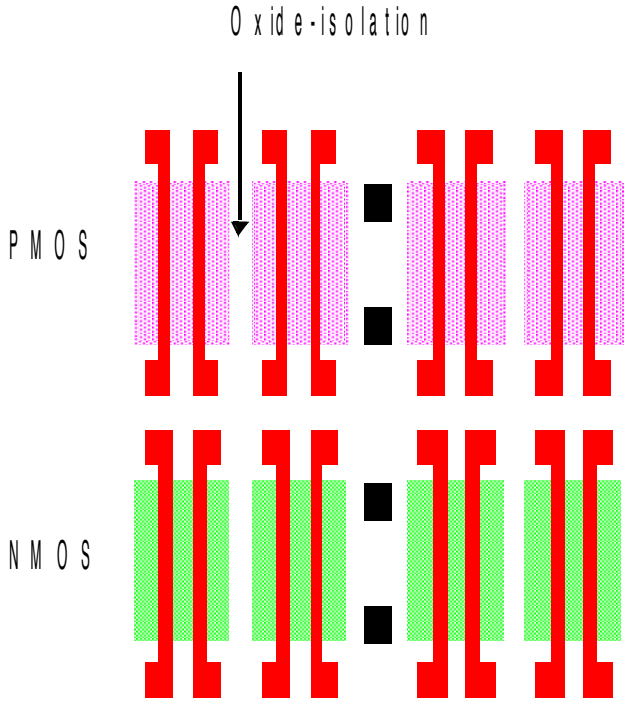


Committed
Cell
(4-input NOR)

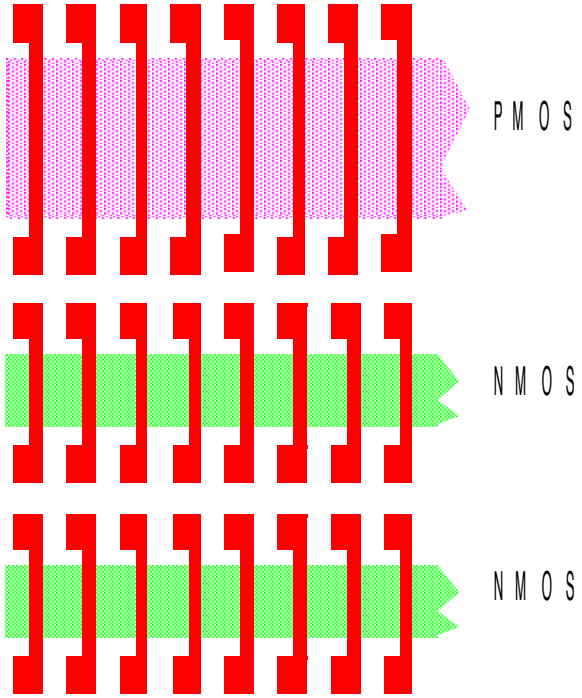
Gate Array Architectures



Examples of Sea-of-gate Primitive Cells

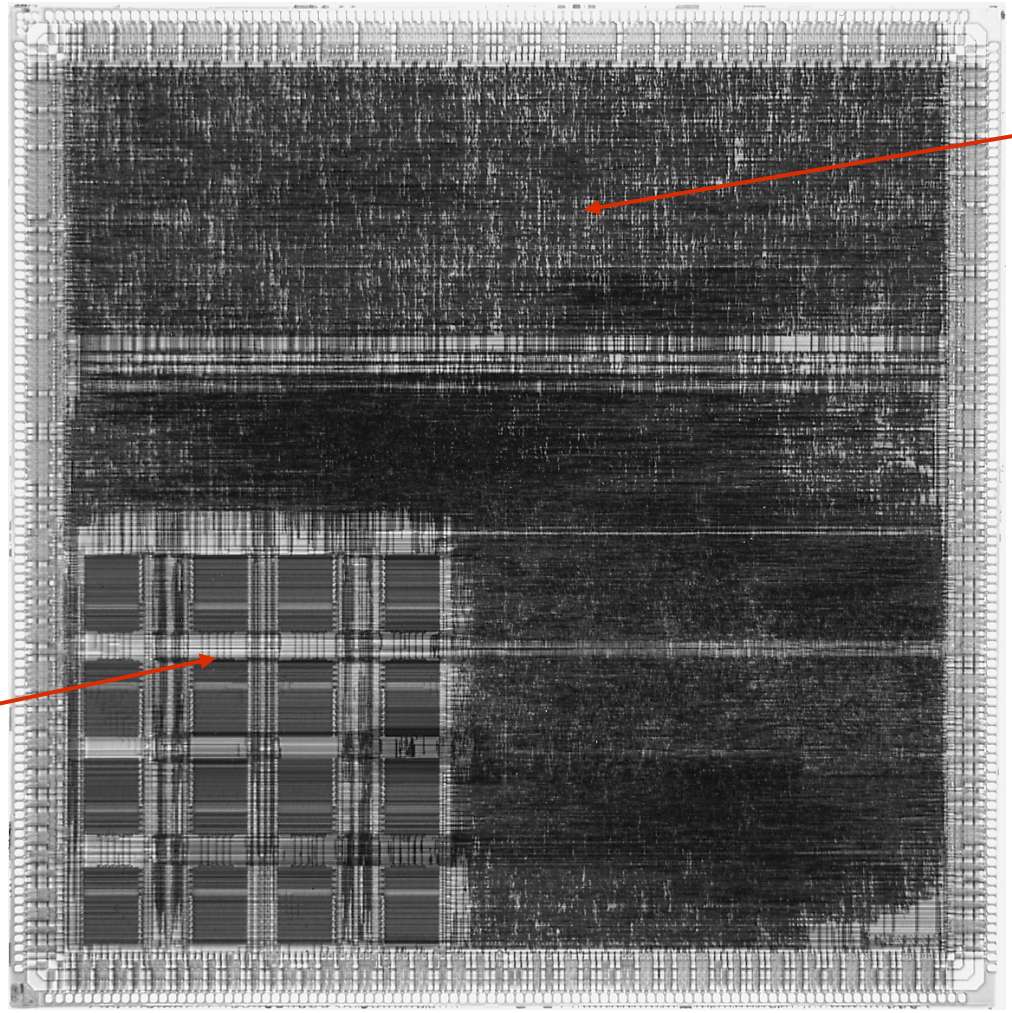


Using oxide-isolation



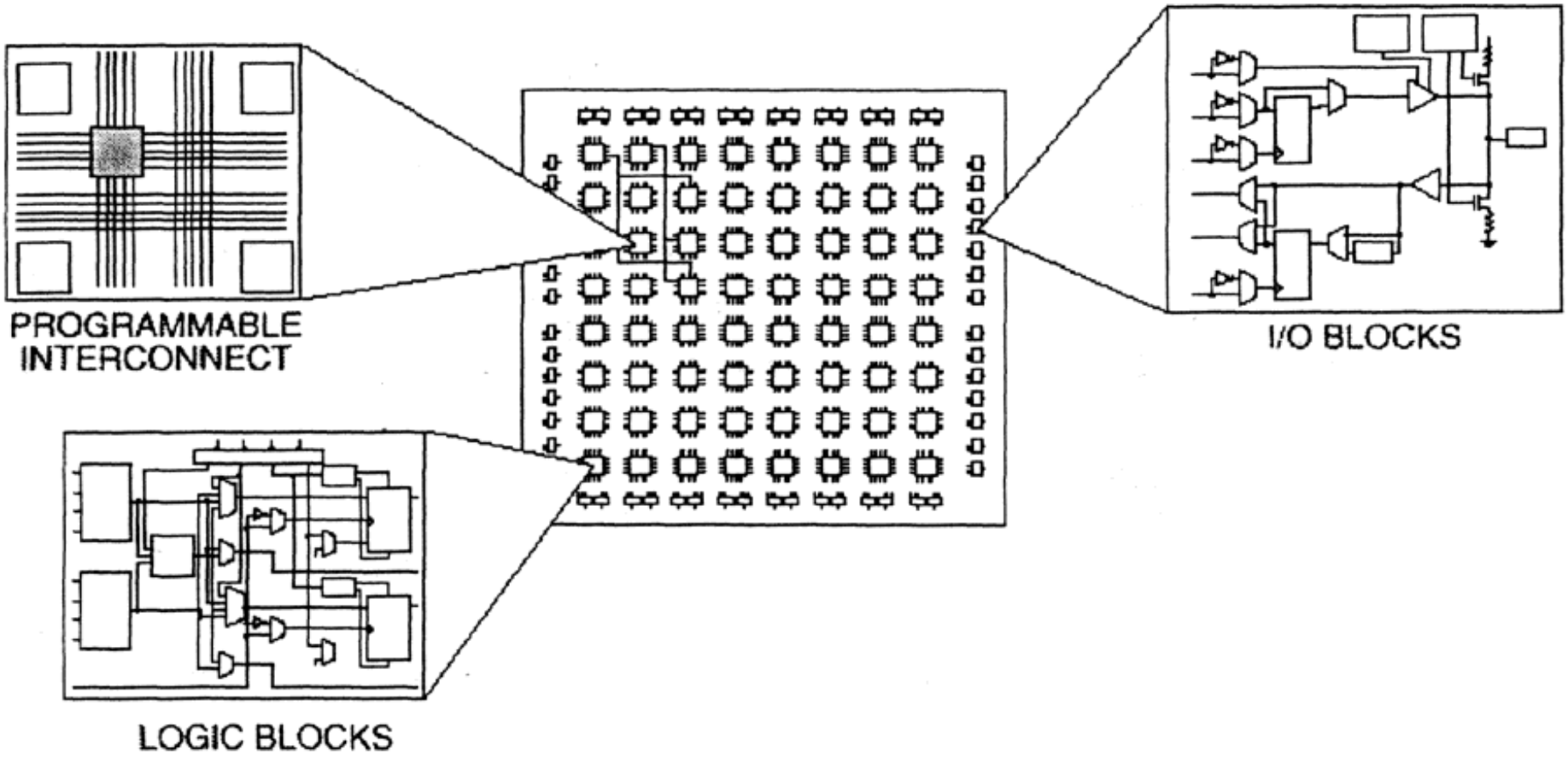
Using gate-isolation

Sea-of-gates

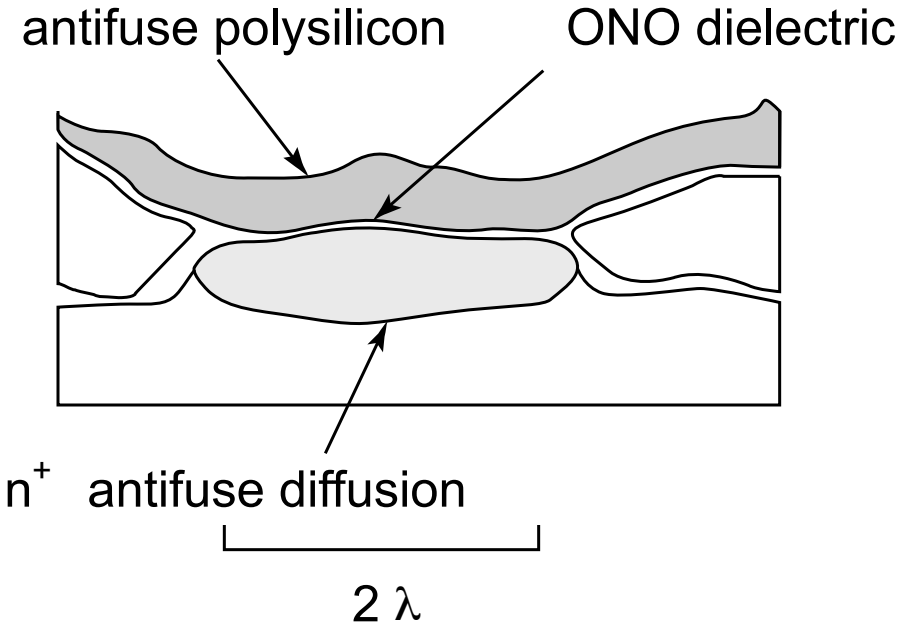


LSI Logic LEA300K
(0.6 μm CMOS)

Xilinx FPGA Architecture

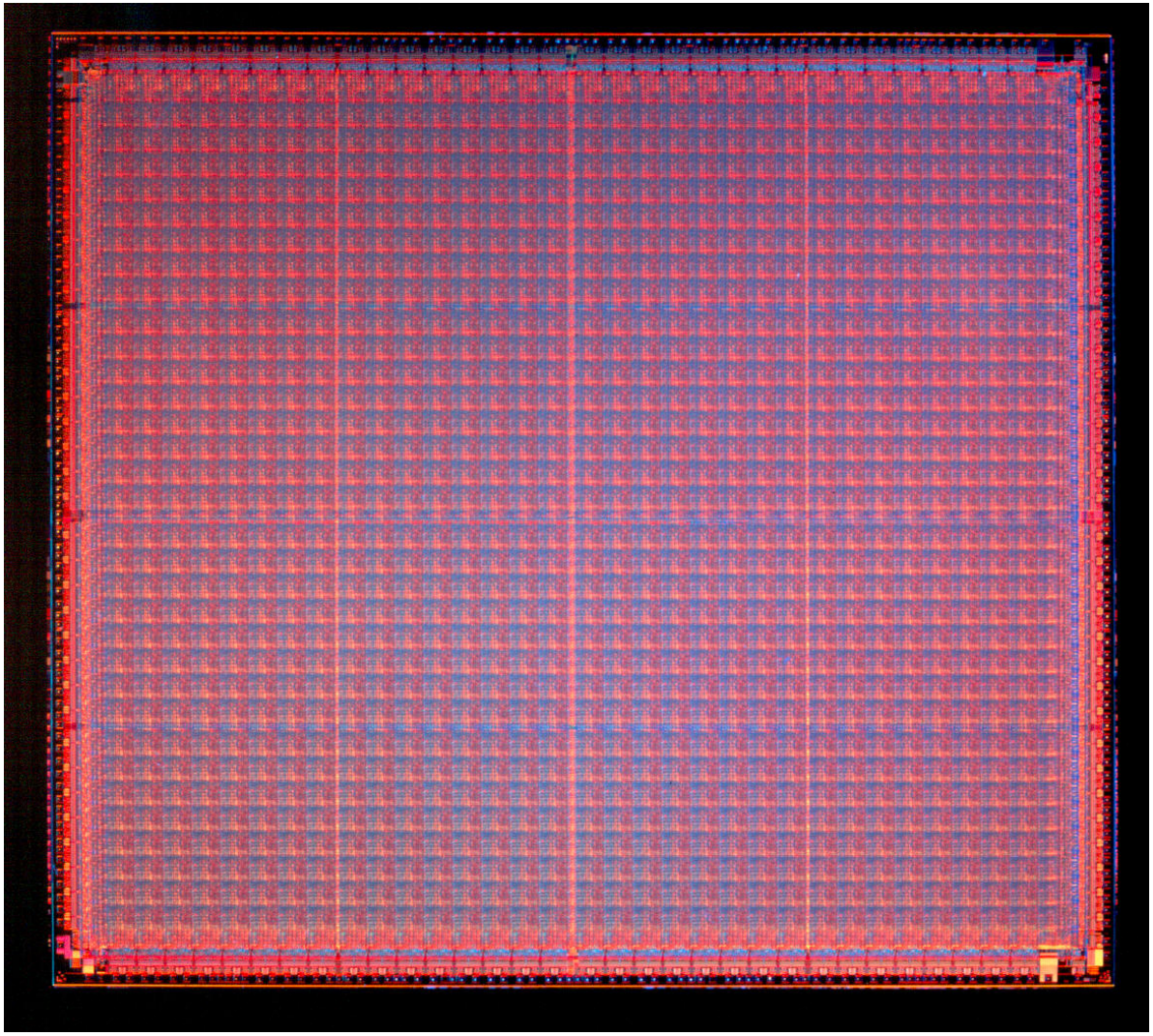


Antifuse-Based FPGA



Open by default, closed by applying current pulse

RAM-based FPGA



Xilinx XC4000ex

Two-Level Logic

$$f_0 = x_0 x_1 + \overline{x_2}$$

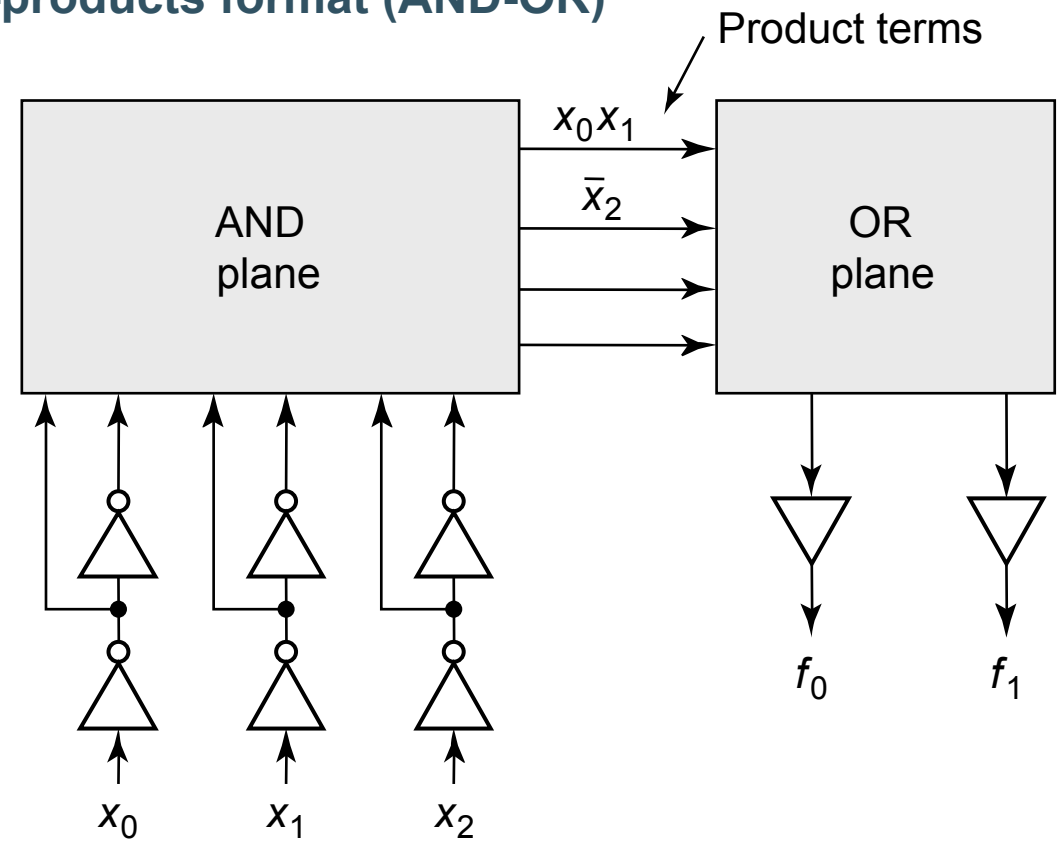
$$f_1 = x_0 x_1 x_2 + \overline{x_2} + \overline{x_0} x_1$$

Inverting format (NOR-NOR) more effective

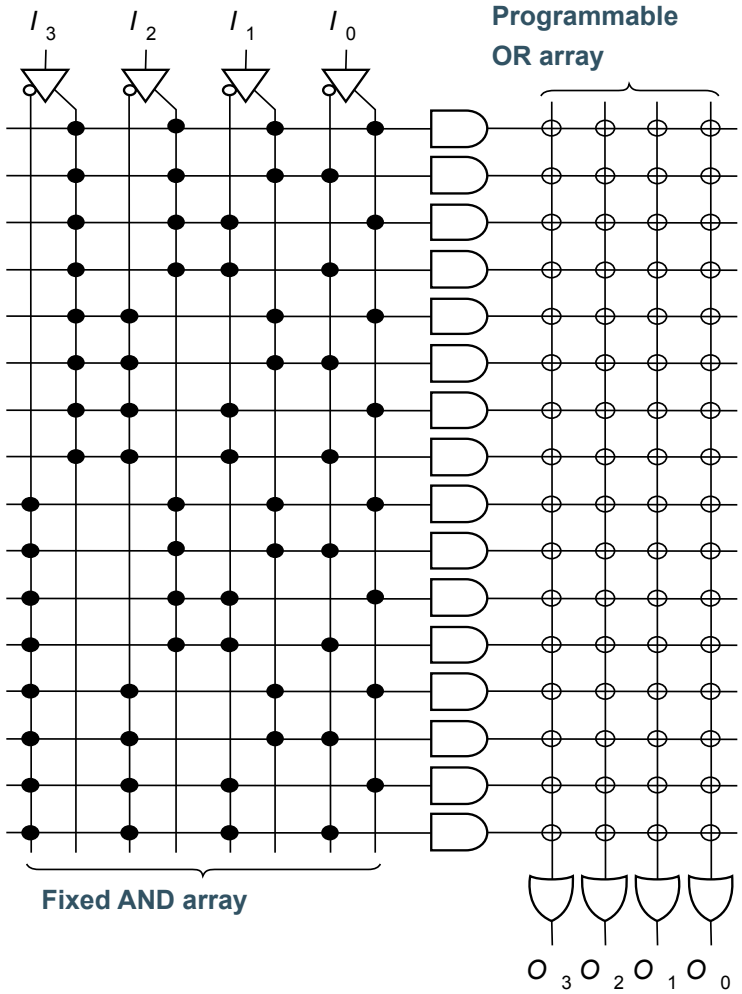
$$\overline{f_0} = \overline{\overline{(\overline{x_0} + \overline{x_1})} + \overline{x_2}}$$

$$\overline{f_1} = \overline{\overline{(\overline{x_0} + \overline{x_1} + \overline{x_2})} + \overline{x_2} + \overline{(x_0 + \overline{x_1})}}$$

Every logic function can be expressed in sum-of-products format (AND-OR)



Array-Based Programmable Logic (1)

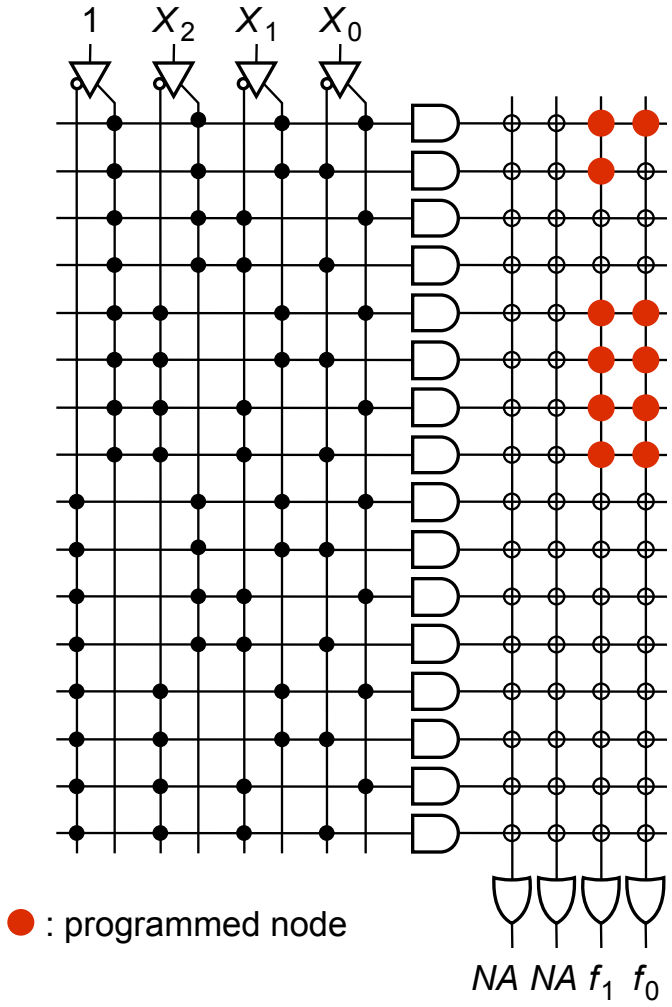


PROM

Indicates programmable connection

Indicates fixed connection

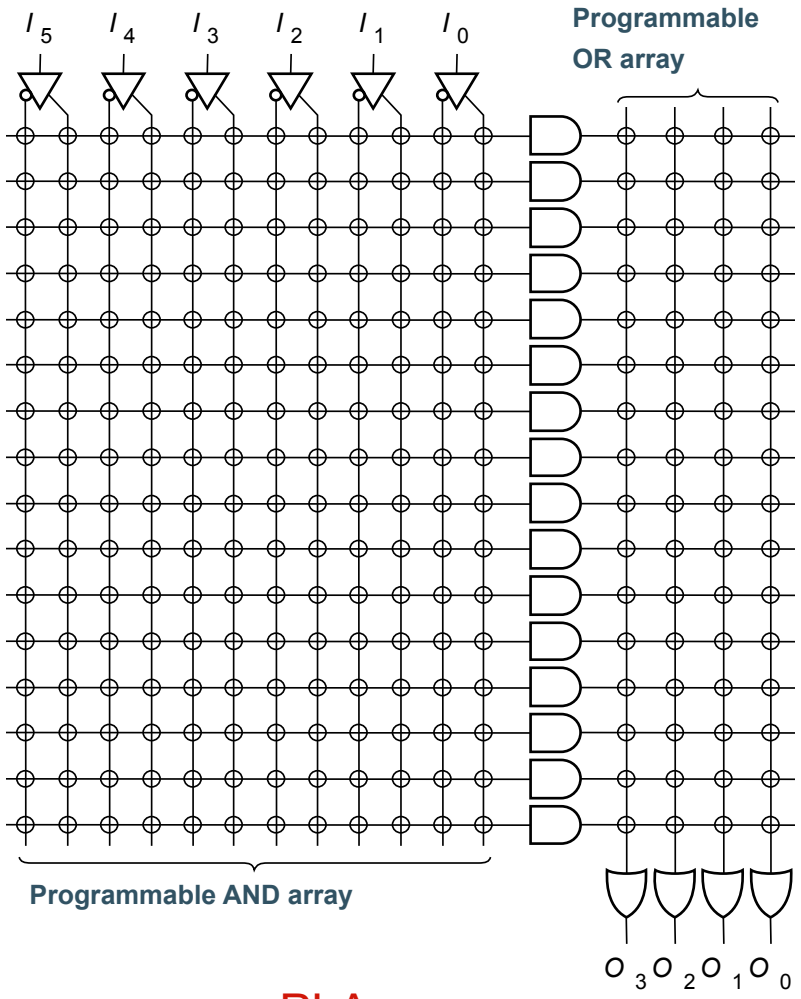
Programming a PROM



$$f_0 = x_0 x_1 + \overline{x_2}$$

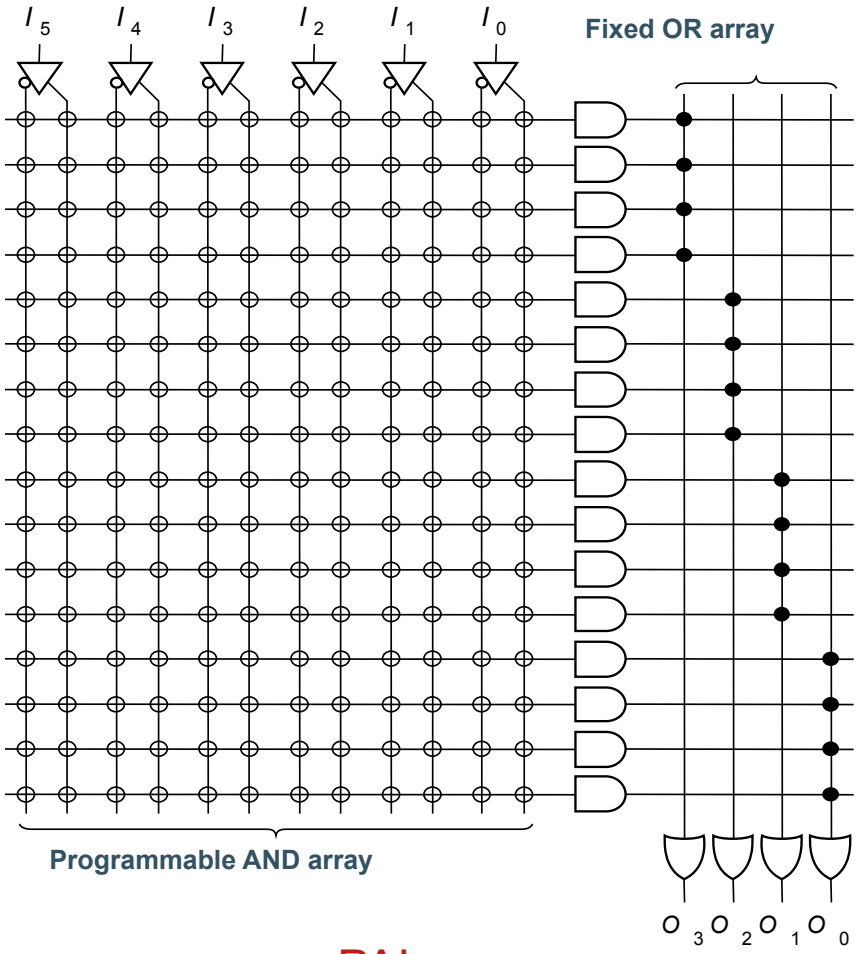
$$f_1 = x_0 x_1 x_2 + \overline{x_2} + \overline{x_0} x_1$$

Array-Based Programmable Logic (2)



PLA

Array-Based Programmable Logic (3)

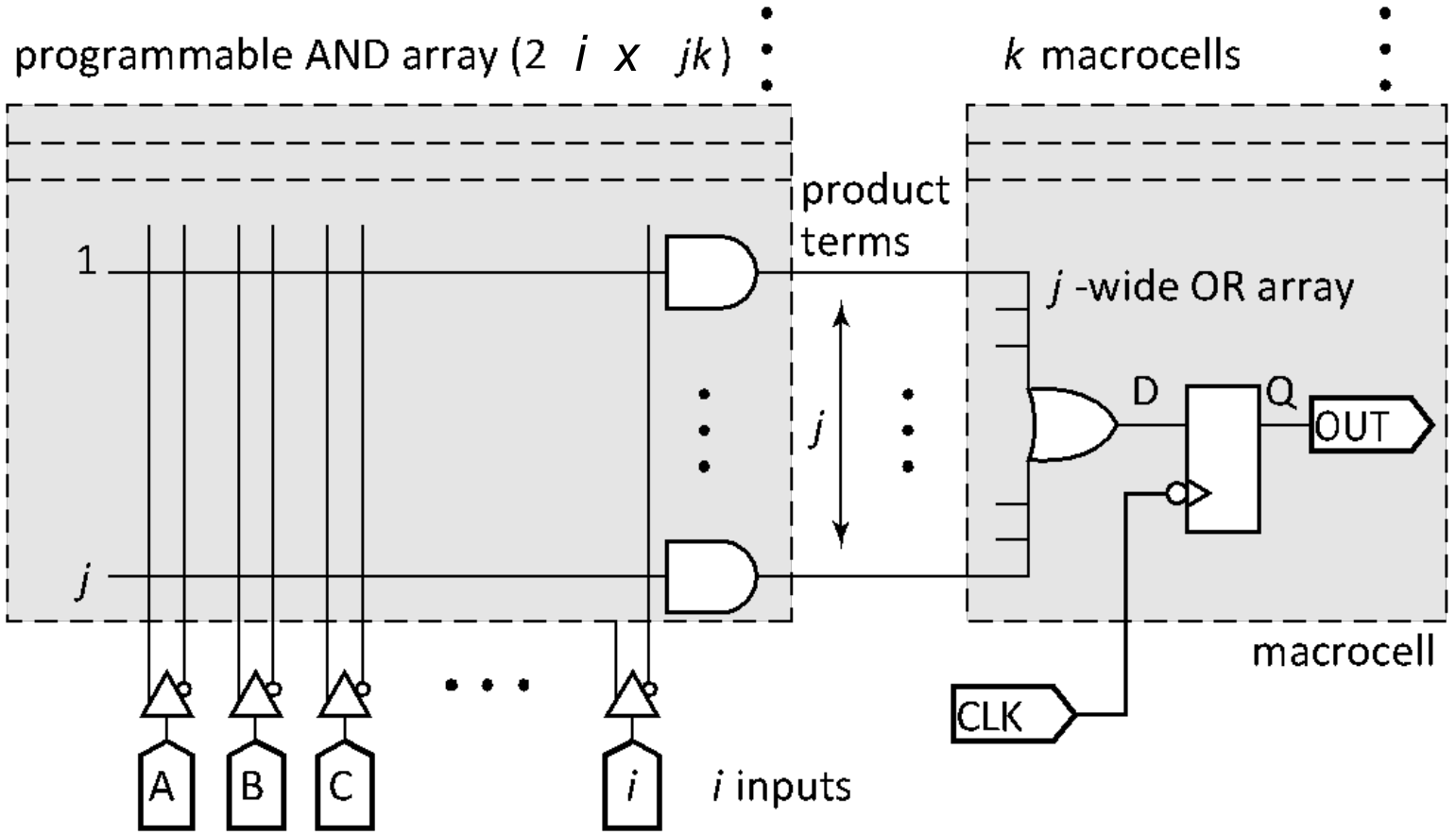


PAL

Indicates programmable connection

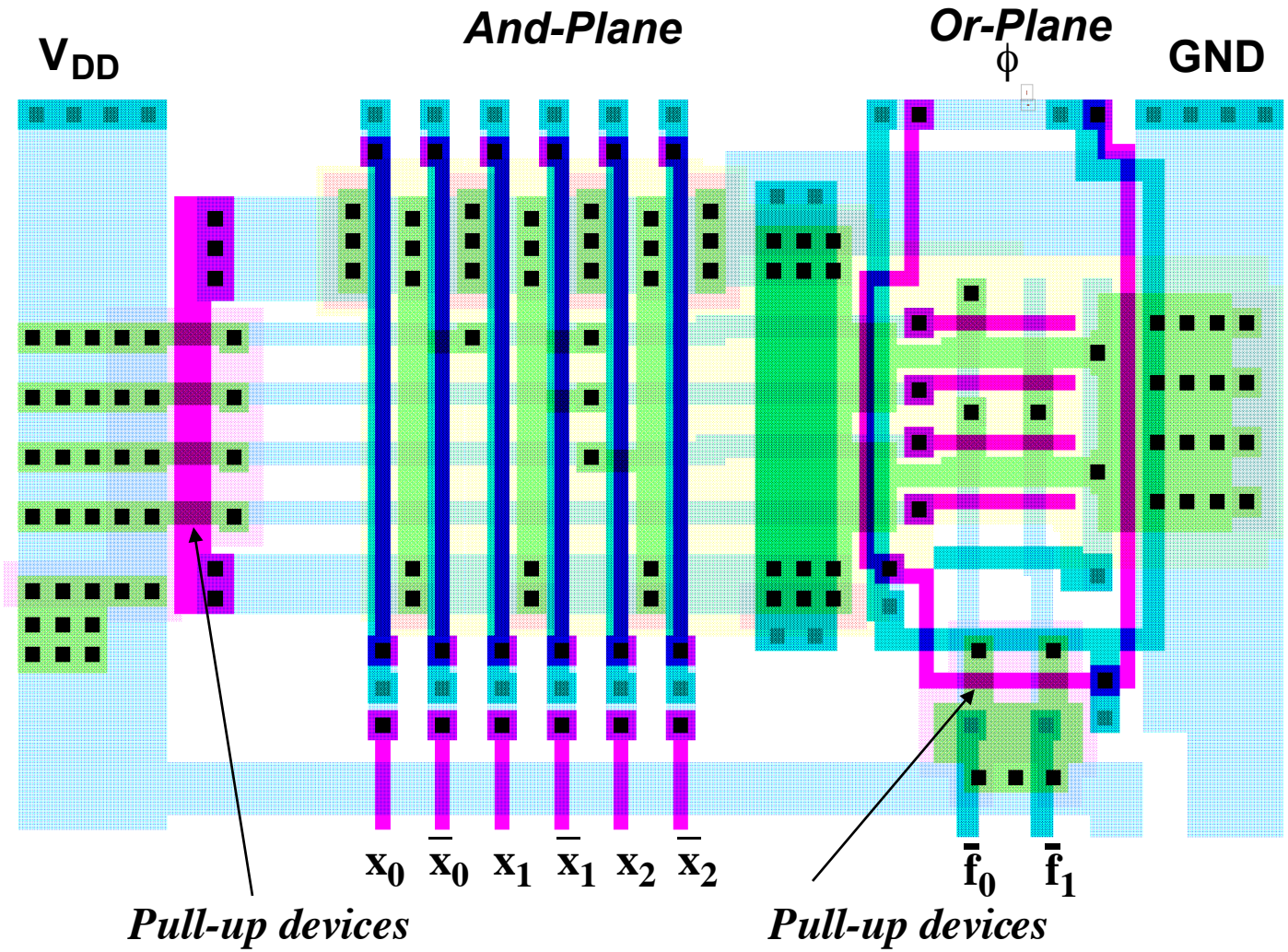
Indicates fixed connection

More Complex PAL

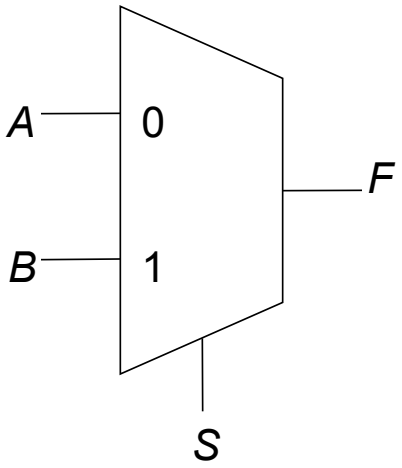


i inputs, j minterms/macrocell, k macrocells

PLA Layout – Exploiting Regularity



Cell-Based Programmable Logic

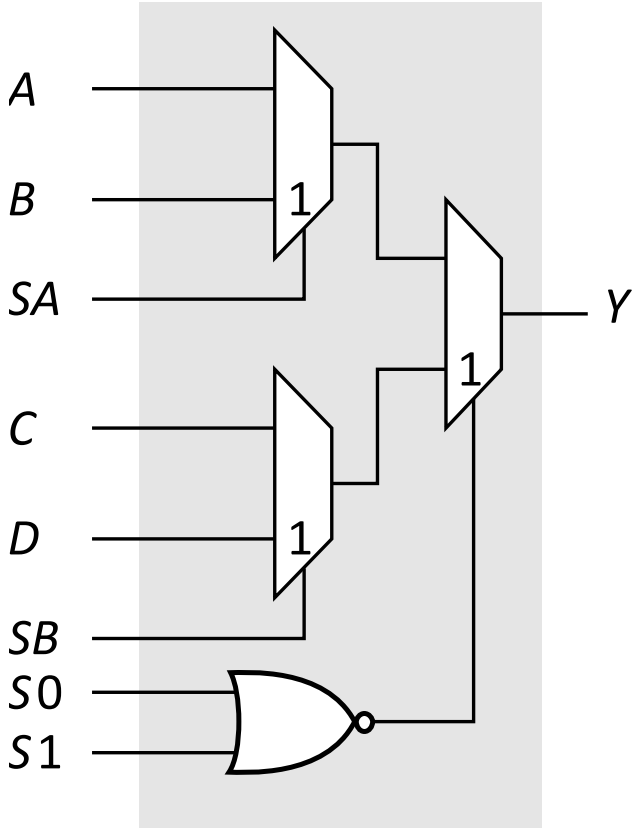


2-input mux as programmable logic block

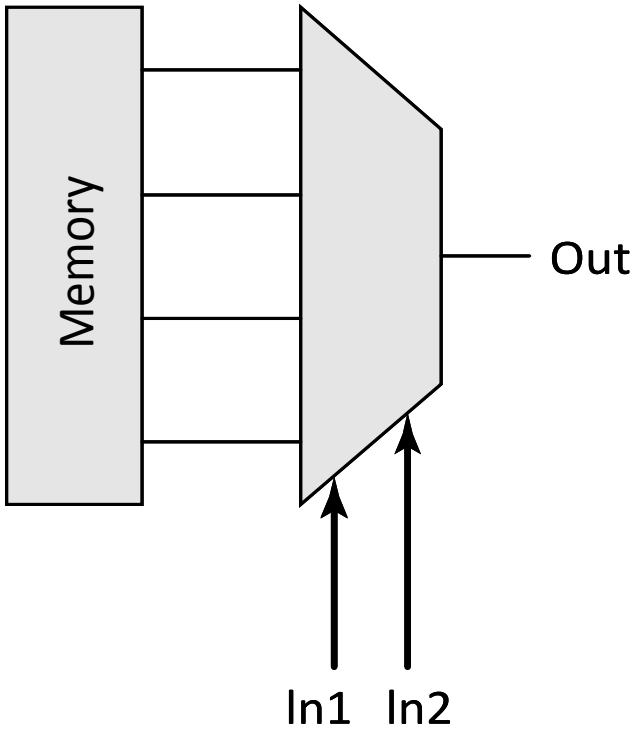
Configuration			
A	***B***	***S***	***F=***
0	0	0	0
0	*X*	1	*X*
0	*Y*	1	*Y*
0	*Y*	*X*	*XY*
X	0	*Y*	$X\overline{Y}$
Y	0	*X*	$\overline{X}Y$
Y	1	*X*	$X + Y$
1	0	*X*	$\overline{X}$
1	0	*Y*	$\overline{Y}$
1	1	1	1

$$F = A \cdot \overline{S} + B \cdot S$$

Logic Cell of Actel Fuse-Based FPGA



Look-up Table Based Logic Cell

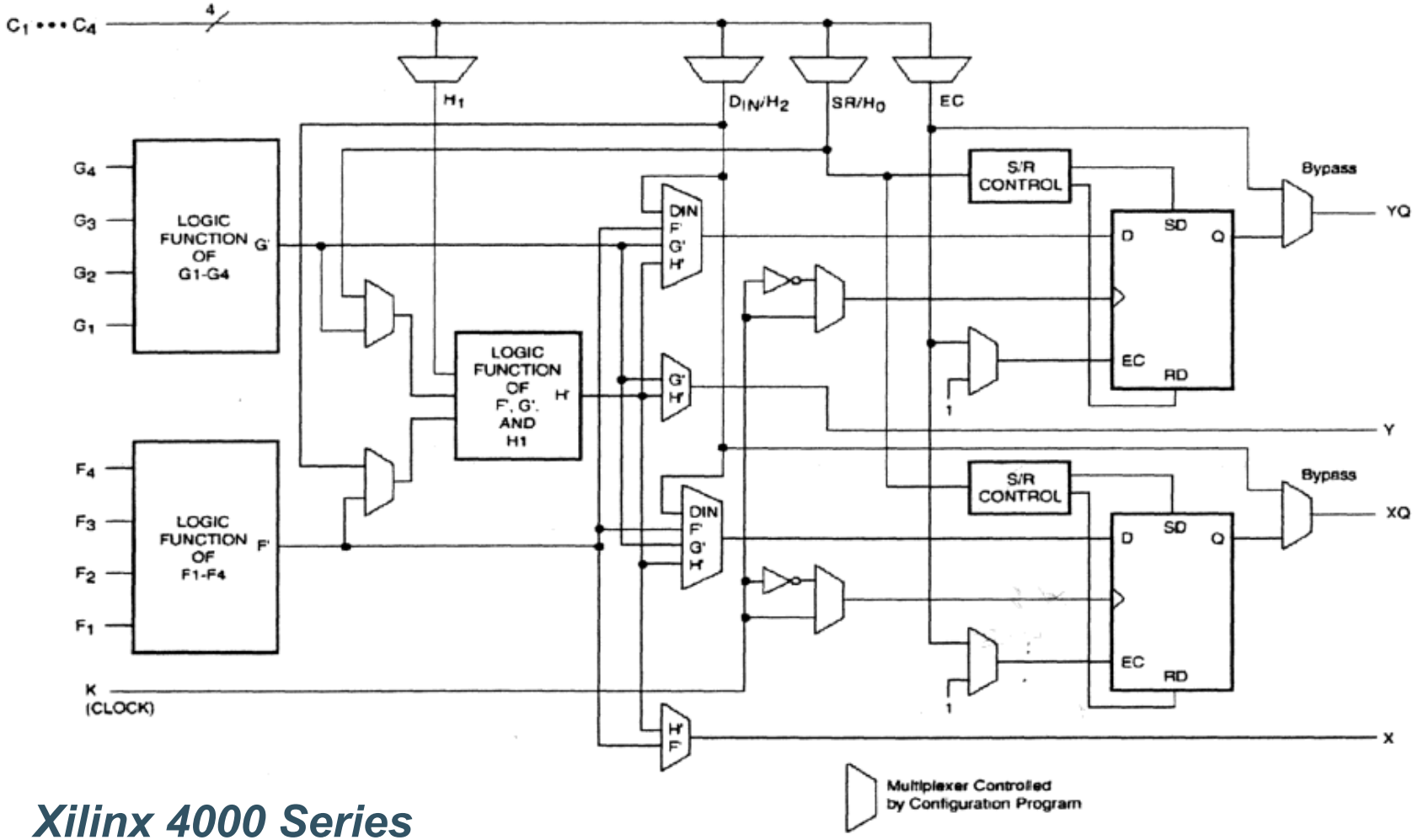


Cell schematic

In	Out
00	0
01	1
10	1
11	0

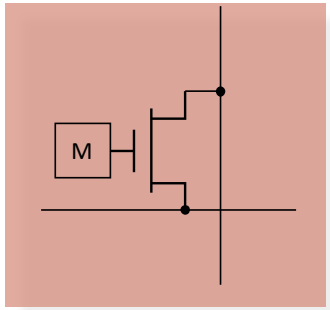
XOR function

LUT-Based Logic Cell

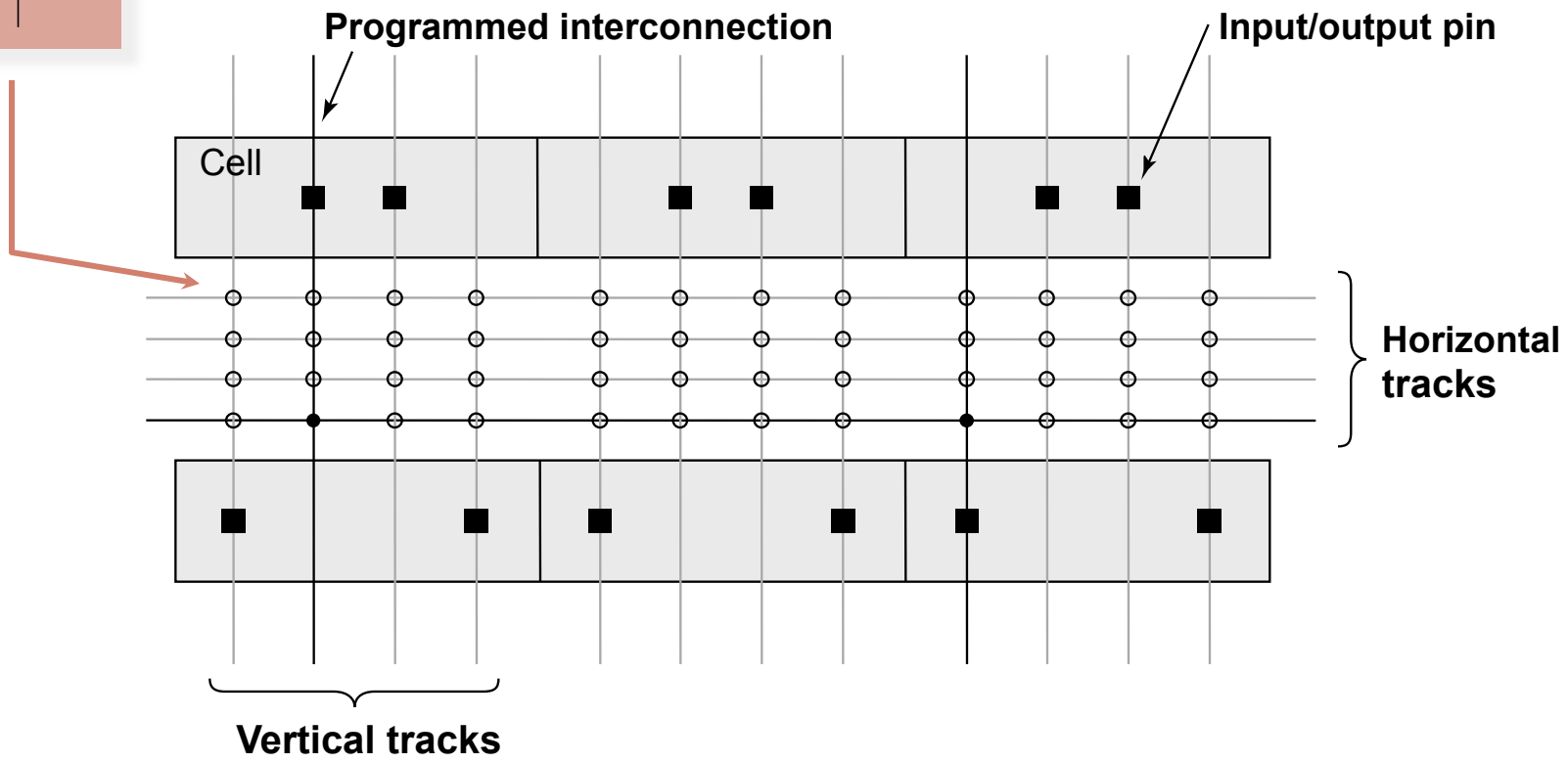


Xilinx 4000 Series

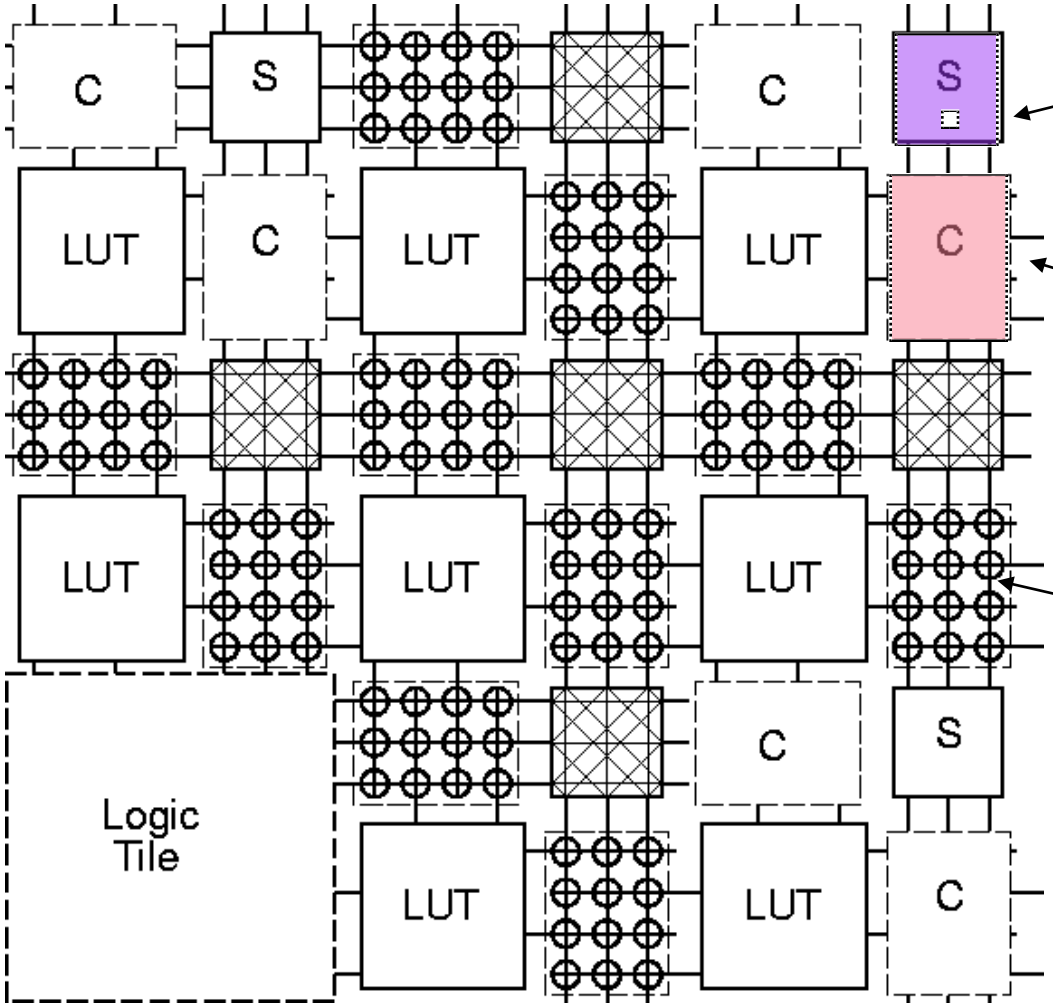
Array-Based Programmable Wiring



Interconnect Point



Mesh-based Interconnect Network

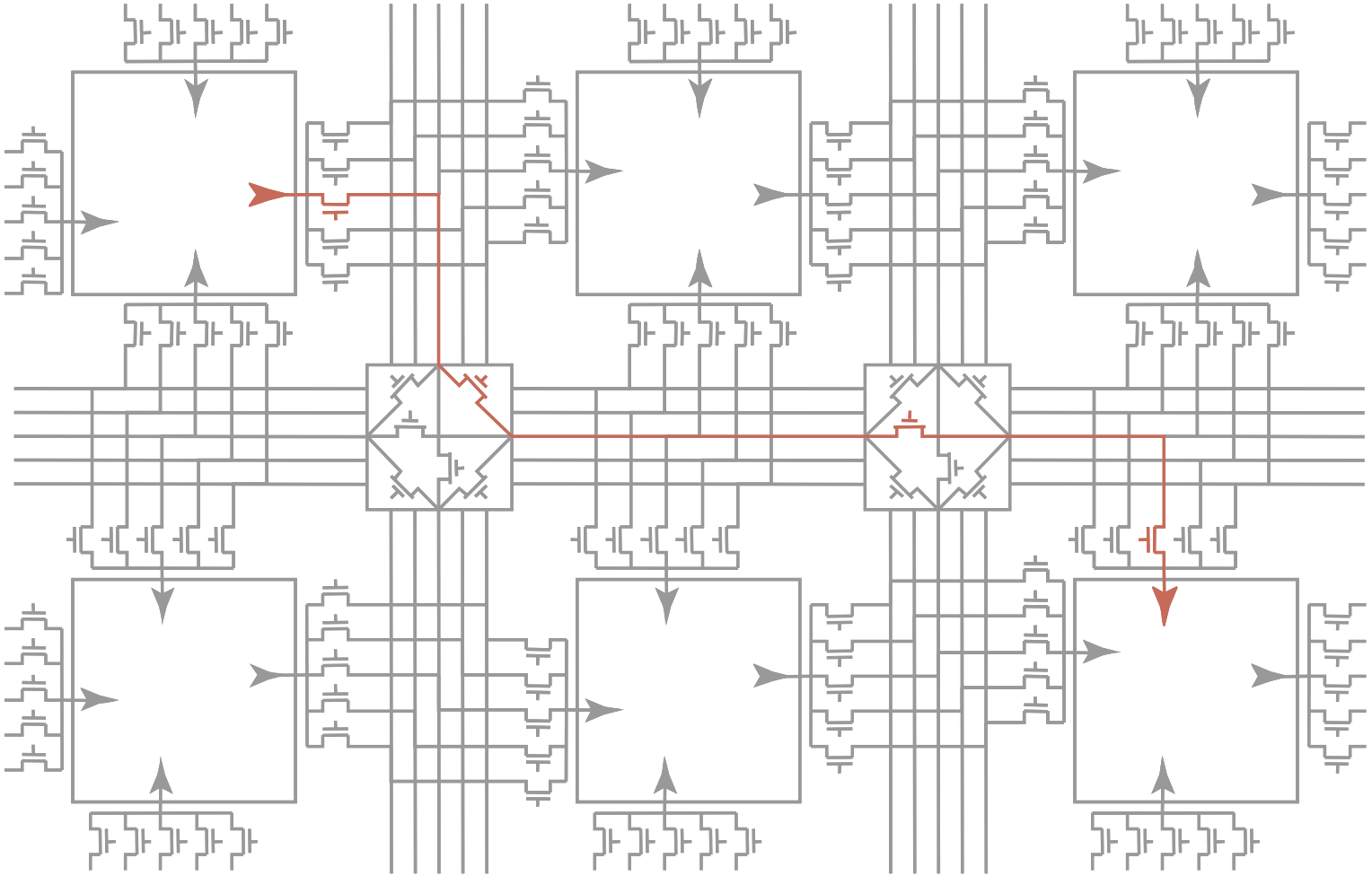


Switch Box

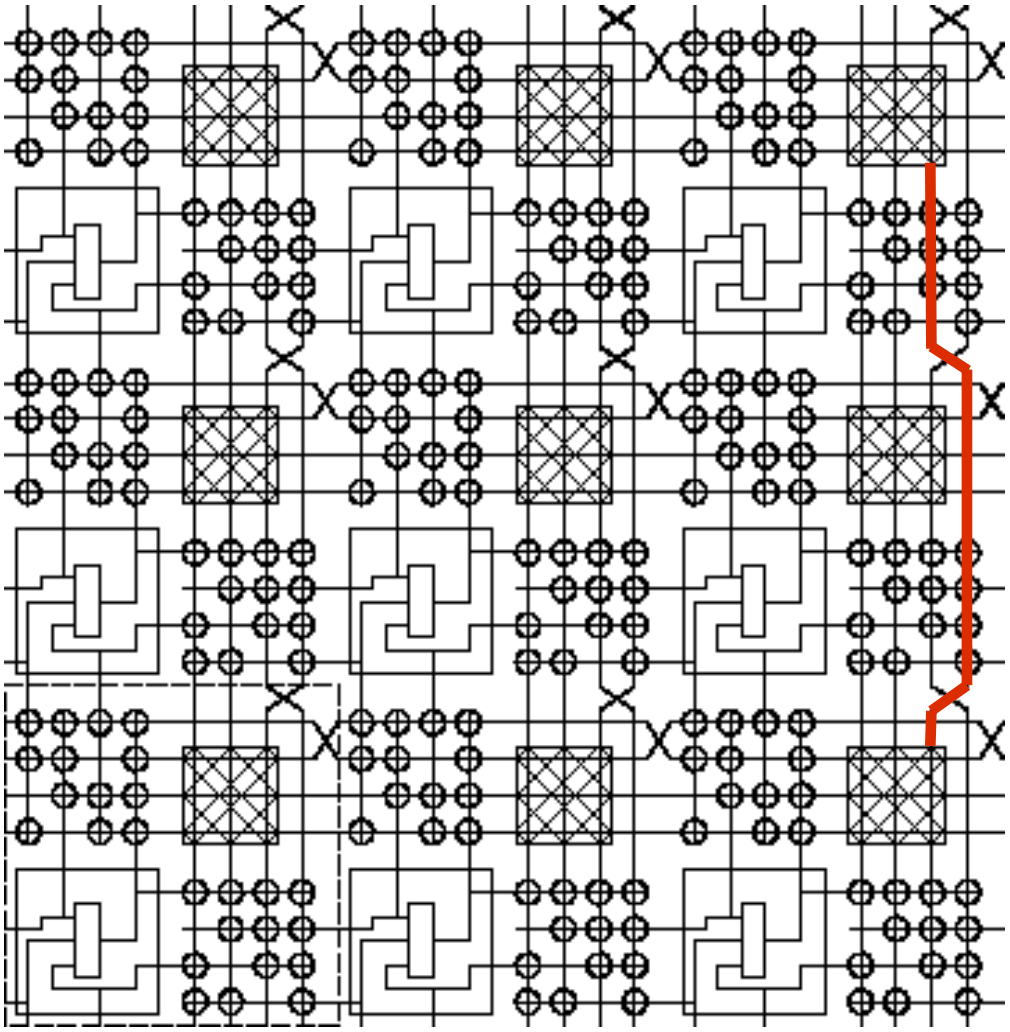
Connect Box

Interconnect
Point

Transistor Implementation of Mesh



Hierarchical Mesh Network



Use overlayed mesh to support longer connections

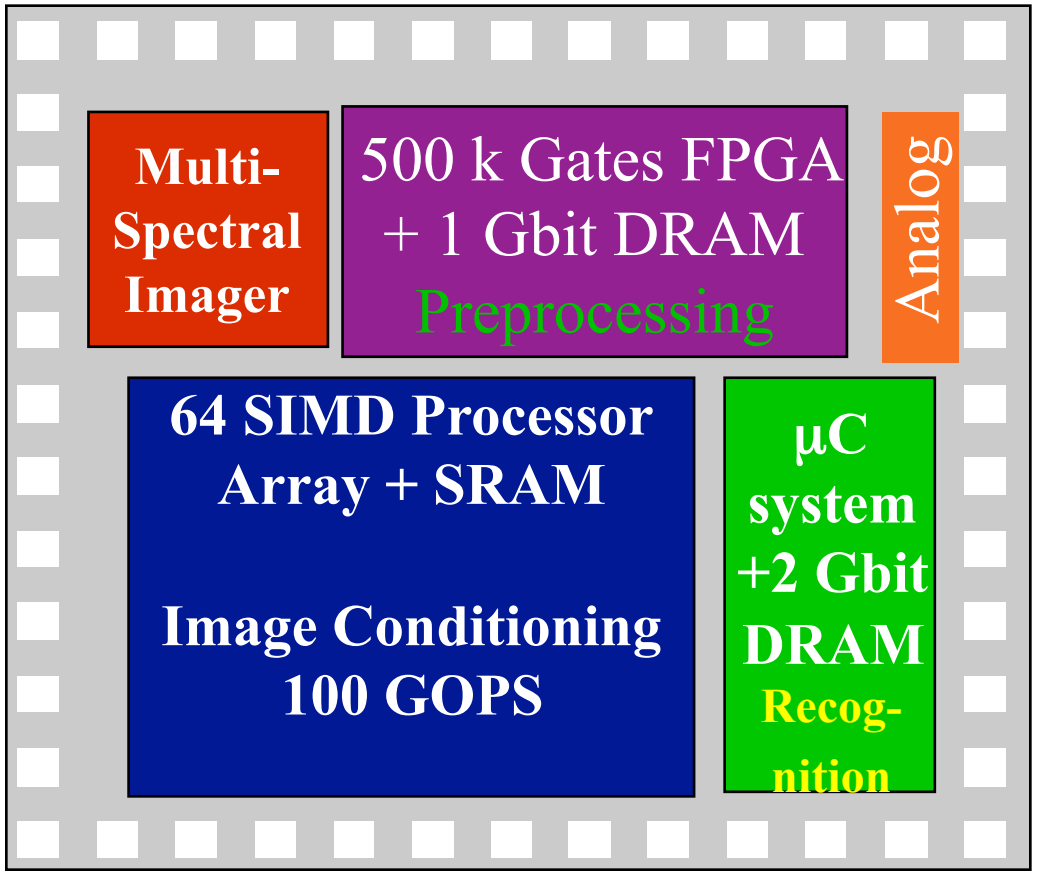
Reduced fanout and reduced resistance

Prewired Arrays

Classification of prewired arrays (or field-programmable devices):

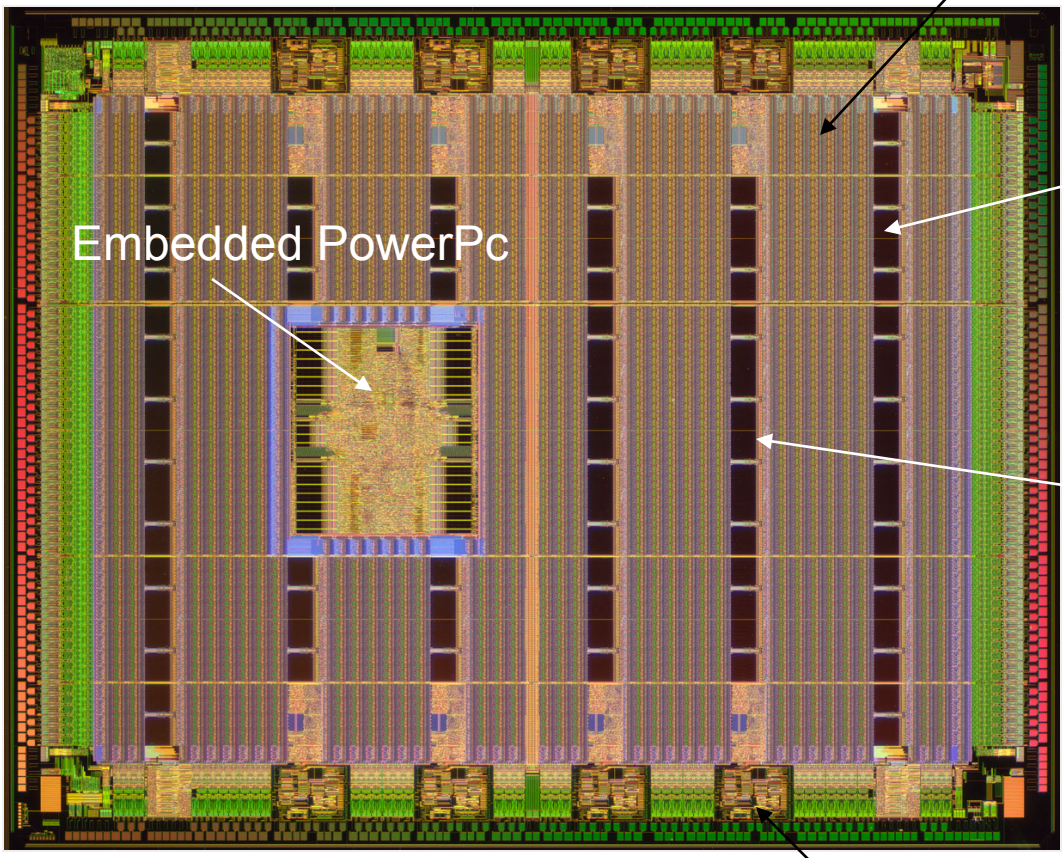
- Based on Programming Technique
  - Fuse-based (program-once)
  - Non-volatile EPROM based
  - RAM based
- Programmable Logic Style
  - Array-Based
  - Look-up Table
- Programmable Interconnect Style
  - Channel-routing
  - Mesh networks

System-on-a-Chip



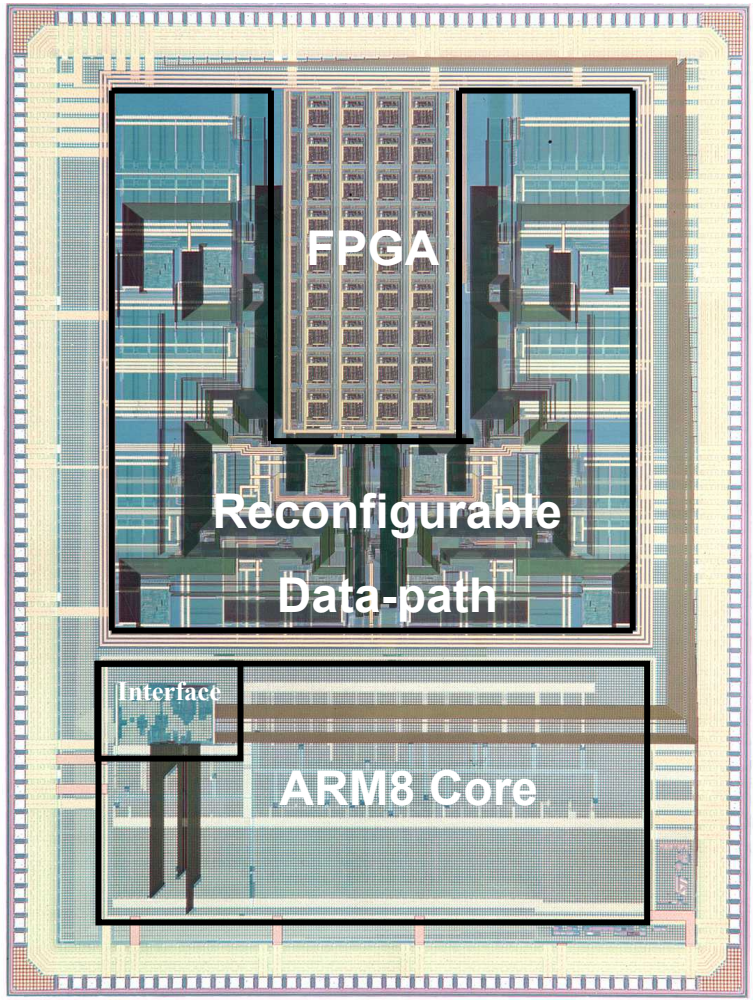
- Embedded applications where cost, performance, and energy are the real issues!
- DSP and control intensive
- Mixed-mode
- Combines programmable and application-specific modules
- Software plays crucial role

Heterogeneous Programmable Platforms



Xilinx Vertex-II Pro

Berkeley Pleiades Processor



- 0.25um 6-level metal CMOS
- 5.2mm x 6.7mm
- 1.2 Million transistors
- 40 MHz at 1V
- 2 extra supplies: 0.4V, 1.5V
- 1.5~2 mW power dissipation

Summary

- Digital CMOS Design is kicking and healthy
- Some major challenges down the road caused by Deep Sub-micron
  - Super GHz design
  - Power consumption!!!!
  - Reliability – making it work

  Some new circuit solutions are bound to emerge
- Who can afford design in the years to come? Some major design methodology change in the making!